THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

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Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract has been to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes have 64 sites, of which eight can be selected for simultaneous use by the external world. On one of the probe designs (PIA-2B/3B), the neural signals are buffered and then passed directly off chip, whereas on the other (PIA-2/-3) the signals are amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) versions of these probes are being developed.

During the past quarter, we have developed a 1.5μm process for polysilicon definition on our recording probes, reducing the previous feature size by a factor of two. This process has been used in a new mask set containing five probes for acute 3-D cell localization and 2-D current source density analysis in visual cortex. Each probe has 54 sites arranged in two or three rows on a single shank less than 215μm wide.

We are continuing our experiments with a variety of site sizes, placements, and coatings in an effort to improve the lifetime of recording sites in-vivo during chronic implants. We are preparing probes to be implanted during the coming quarter with various biopolymers, including electrodeposited polypyrrole/peptide CDPGYIGSR a neuronal binding agent), PEG (polyethylene glycol, to decrease protein adsorption and cell attachment), and PEDOT (poly(3,4-ethylenedioxythiophene), which is a conducting polymer based upon thiphene. During the past quarter, two chronic probes have been implanted with a variety of site positions on the substrate and with site areas of 1000μm^2 at the tip and 177 μm^2 near the center of the substrate. Currently, the probes have been implanted for eight weeks and two weeks in two different animals. All sites on both probes are currently active, with evidence of single-unit, multi-unit and/or evoked potential activity on every channel. Standard methods are being developed to analyze these waveforms so that differences in site recording capability can be compared from probe to probe and animal to animal. The waveforms are thresholded to extract spikes that exceed four standard deviations above the total signal average (spikes plus noise). A cluster plot is then constructed using the first two principal components of the total separated spikes, and k-means clustering is used to separate the spikes into single units and eliminate spikes likely to have been caused by noise. Finally, a template (average) waveform is constructed for each separated single unit. The signal-to-noise ratio (SNR) is then defined as the peak-to-peak voltage of the template waveform to the standard deviation of the neural record with spikes extracted. For the two probes implanted thus far, the SNRs for tip sites and center sites have been 6.6 and 6.4 for the day of implant, respectively, and 5.9 and 4.7 eight weeks after implant. The increased noise seen over time appears to track well with the increase in the real part of the site impedance.

In developing active probes, two new mask sets containing a variety of active probes are now in fabrication. These include a redesigned PIA-2B/-3B as well as probes containing readout circuits that will be used on PIA-2/-3 later this year. The circuits being evaluated on these probes include several amplifiers having gains of approximately 1000 from 10Hz to >10kHz, zero or unity DC gain, power dissipation of <100µW, and areas of <0.1mm^2. The input-referred noise on these circuits is typically less than 7µV-rms. In addition, multiplexer designs are being evaluated. MOSIS chips with the first of the telemetry interface designs were received during the past term and were evaluated. In spite of the fact that the PMOS device thresholds were larger than the design targets provided initially by the foundry, several of these circuits functioned nearly as expected. The circuits have been redesigned to make them more tolerant to process-induced variations and have been resubmitted for fabrication. The are expected back this fall, when they will be evaluated.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the preserving the viability of the sites in-vivo (preventing tissue encapsulation of the sites) and with the probe output leads, both in terms of their number and their insulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the meg-ohm impedance levels of the sites while maintaining lead flexibility.

Our solution to the lead problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of over 100, impedance levels are reduced by three to four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing has

been developed (PIA-2B) along with a high-end multiplexed probe that includes gain (PIA-2). During the past quarter, we have continued work to understand the chronic behavior of thin-film recording sites and its relationship to site position and design. Standard analysis procedures have been defined for evaluating recording performance and have been applied to probes implanted for as long as eight weeks. A variety of new readout circuits have been designed for the active recording probes and are in fabrication. Finally, telemetry interface circuits fabricated by MOSIS have been evaluated, iterated, and resubmitted for additional fabrication. Work in these areas is discussed in the following sections.

2. Passive Probe Development

The Center for Neural Communication Technology continues to distribute passive probes to users both internal and external to the University of Michigan based on technology developed as the result of NINDS contracts. Among the recent recipients of probes are Neural Prosthesis Program investigators Dave Edell of InnerSea Technology, Daryl Kipke of Arizona State University, and Bill Agnew, Doug McCreery and Leo Bullara of Huntington Medical Research Institutes. In addition to distributing standard passive devices, the CNCT fabricates custom probes for experienced users and collaborators. During the last quarter, a new mask set was fabricated to completion. "SMALLFEATURES" was designed with CNCT collaborators Tim Blanche, Phil Hetherington, Ph.D., and Nicholas Swindale, Ph.D., of the University of British Columbia. This mask set incorporates smaller-than-usual minimum feature sizes (1.5µm space and trace as compared to the 3µm typically used for passive probe polysilicon interconnects) to realize higher density, single-shank probes. The small traces were successfully defined using a Lam TCP9400 etcher that is specifically designed for etching polysilicon. This reactor was purchased two years ago and will increasingly be used as part of probe fabrication.

The five probe types on the mask were designed for acute 3-D cell localization and 2-D current source density analysis in visual cortex. Each probe has 54 sites arranged in two or three rows on a single shank that is less than 215µm wide. The design shown in Fig. 1 has three rows of staggered sites that are spaced at 65µm in the vertical dimension. Figure 2 shows the tips of all five designs, and Fig. 3 shows close-ups the recording sites and polysilicon traces. AC impedance tests have been performed on these probes and the sites are acceptable and consistent. A PC board/connector is currently being designed in collaboration with UBC and Casey Stengel of Neuralynx, Inc.

3. Chronic Implants with Passive Recording Probes

3.1 Chronic Animals

A number of strategies are being pursued in the search for an extension to the useful life of chronic recording electrodes. All aspects of our probe development

program are involved, including the Neuroprosthesis Program projects, CNCT, and our collaboration with the University of Michigan Material Science and Engineering Department. Hypotheses exist which envision either adsorption of proteins on the electrode site or the active formation of a gial layer over the sites. Our work suggests the former, but there is some evidence that a gial layer can form when the probe surface is not cleaned properly or when there is excessive damage due to the implant surgery. The strategies are: 1) disruption of the surface obstruction by electrical current flow, 2) cleaning of a convex metal site surface by exposure to motion of the tissue around the site, 3) prevention of protein adsorption through chemical coatings, and 4) actively encouraging nerve cells to associate with the probe sites. Only the last method is specific to improving the connectivity to nerve cells but all of the methods have shown promise at some level at achieving success. We will continue to experiment with all of these methods until one or a combination shows distinct superiority.

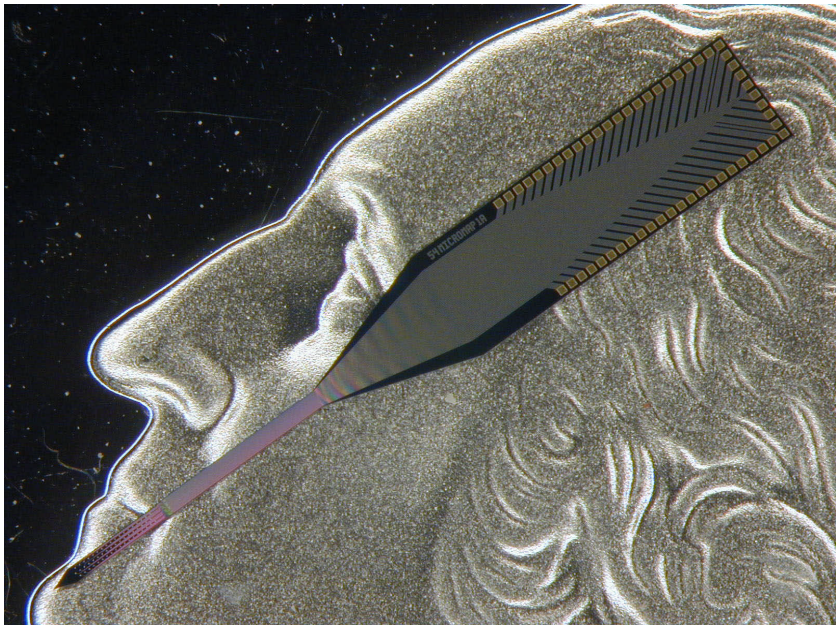


Fig. 1: New 54-channel probe design fabricated for UBC on the head of a quarter. Probes on this mask set have 1.5µm polysilicon features to permit high channel counts on shanks less than 215µm wide. The total length of this design from tip to backend is 1.06cm.

During the next quarter we will implant one of the tip-site probes that will be rigidly mounted to the connector to better mimic a true microwire electrode. We will also implant some of the new side-site probes, which unlike our previous side site probes have the sites extending off the edge of the probe to varying degrees. Two sites of this type are shown in Fig. 4.

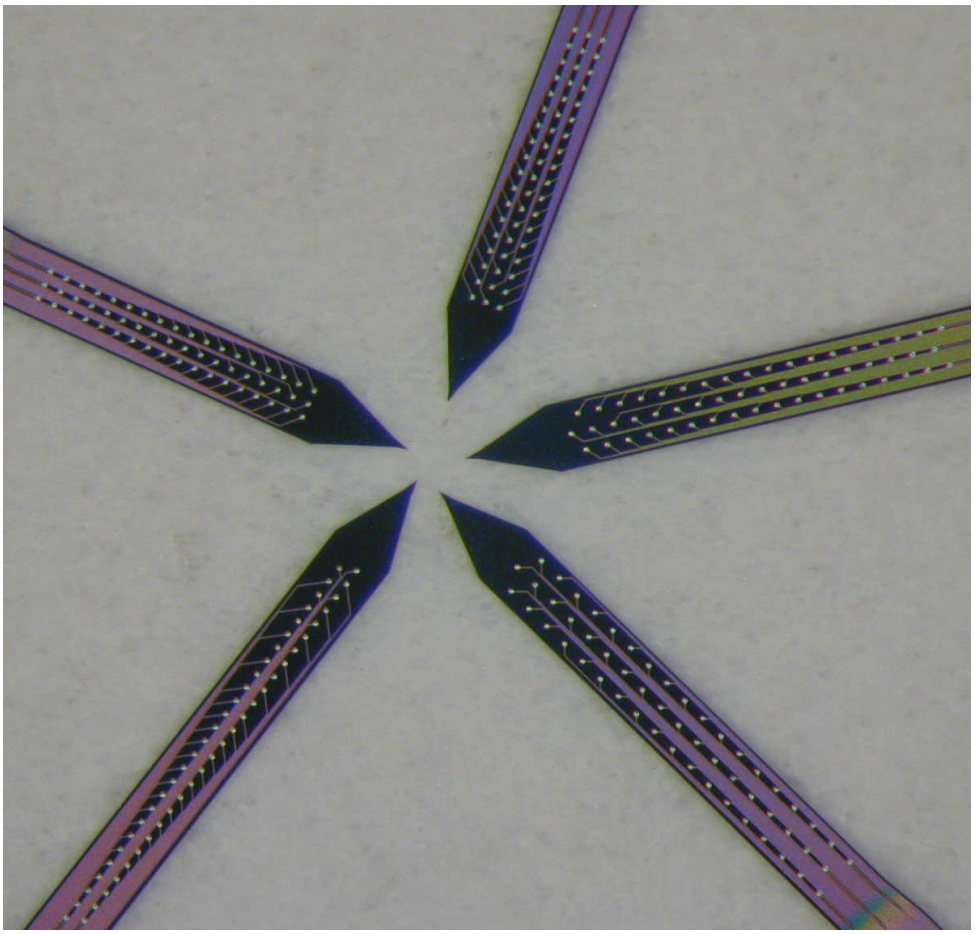


Fig. 2: Tips of the five designs on the "SMALLFEATURES" mask set. These 54-channel probes were designed for 3-D cell localization and 2-D current source density in cortex. Shank widths range between 200 and 212µm.

3.2 Electrode Coatings

During the coming quarter, we will implant chronic probes that will have sites coated with various biopolymers. The first such device will have sites electrodeposited with polypyrrole/peptide CDPGYIGSR. The peptide is a laminin fragment, is able to bind to neurons and is found in many extracellular proteins. The rationale for this approach is to encourage the nerve cells to associate more closely to the sites, thus making their electrical activity more visible to the site. The second experiment will involve PEG (polyethylene glycol). This coating is not electrodeposited and therefore is not site specific. PEG will be applied to the entire probe structure. PEG has been shown to promote decreased protein adsorption and cell attachment. It is thought to do this as a result of an entropic effect generated by the structure of the polymer, which is brush-like. The third probe type will be coated with PEDOT (poly(3,4-ethylenedioxythiophene)), which is a conducting polymer based upon thiphene.

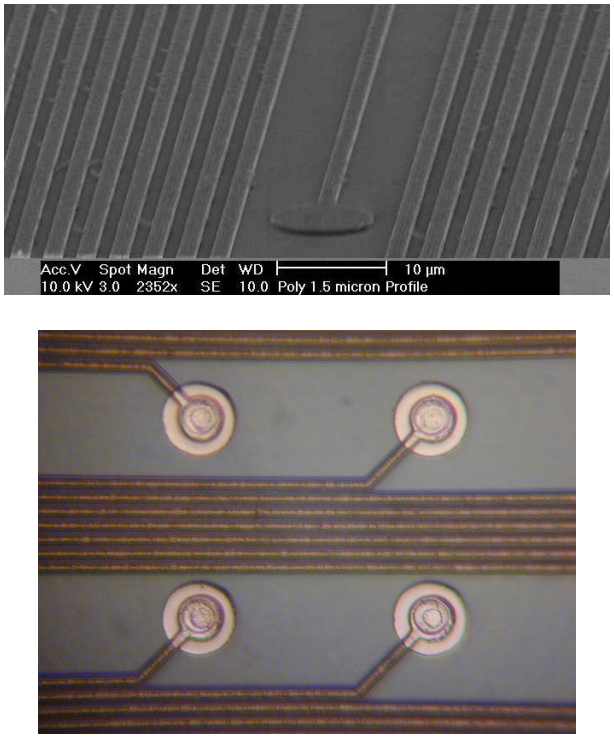


Fig. 3: SEM of a partially fabricated device (left) and high magnification photograph of a completed device. The pitch (line plus space) of the polysilicon leads is 3µm. On the right, sites are spaced at 50µm.

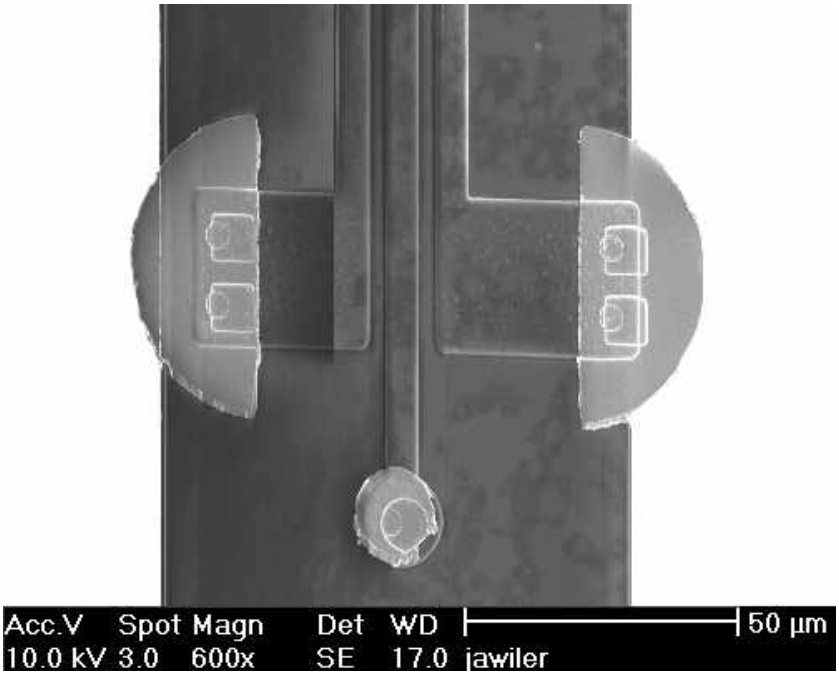


Fig. 4: SEM of a probe shank containing sites that overlap the edge of the substrate as well as a site centered on the shank.

3.3 Tests of Probe Cleaning Procedures

During this past quarter, we implanted the LTO and CVD four-shank electrodes which have been ultra cleaned, as described in the previous quarterly report. The animals have been sacrificed, and we are waiting on the histological analysis.

4. Chronic Recording

4.1 Silicon "Microwire" Implants

During the past quarter, two chronic recording probes were implanted in guinea pig auditory cortex. These are the first of a series of implants that will address questions regarding the nature of the tissue/electrode interface and the viability of long-term recordings. We will determine the baseline longevity and stability of chronic cortical recordings with these probes and explore the hypothesis that the mechanical cleaning of sites due to small electrode movements contributes to longer periods of successful recording.

The probes have sites that are likely to be exposed to small tissue movements due to their location at the shank tip (Fig. 5). The probes have integrated silicon ribbon cables bonded to sixteen-channel Omnetics percutaneous connectors. These experiments will also provide additional chronic testing of the silicon ribbon cables. In addition, the implants will provide useful information about experimental procedures in chronic preparations.

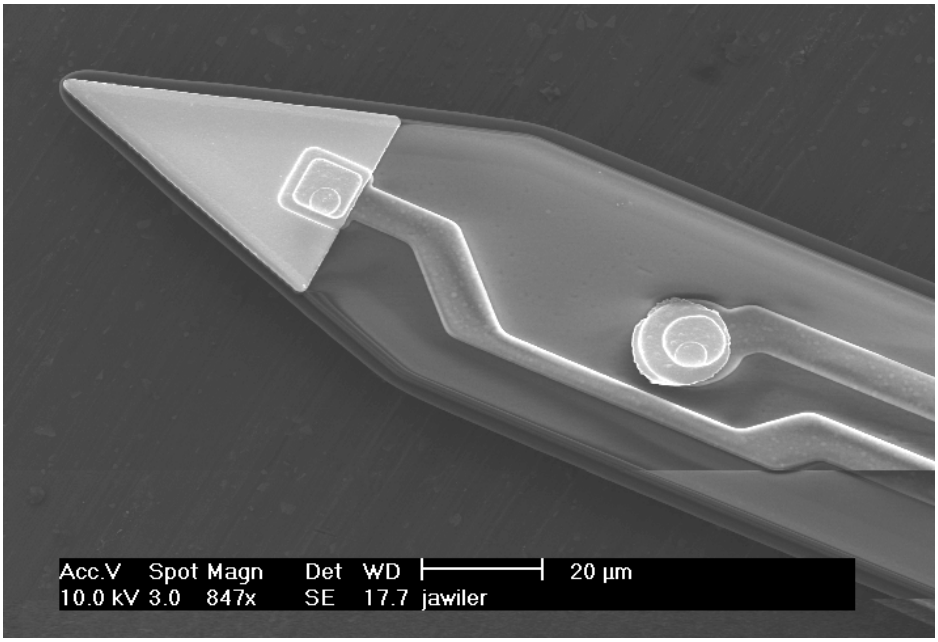


Fig. 5: Scanning electron micrograph of the tip of a chronic probe. The large tip site is roughly 1000μm^2, while the smaller round site is 177 μm^2.

Currently, the probes have been implanted for eight weeks and two weeks, respectively, in two different animals. All sites on both probes are currently active, with evidence of single-unit, multi-unit and/or evoked potential activity on every channel. Figure 6 shows 100msec of activity on one of the channels of the implant after eight weeks of implantation.

4.2 Characterization of Chronic Implants

The characterization and quantification of recording performance during chronic implantation are paramount in seeking to evaluate different designs en route to a long-term chronic implant. The analysis of electrode performance by researchers utilizing chronic multi-channel recording tends to be somewhat subjective and anecdotal. Even a seemingly simple measure such as signal-to-noise ratio can be construed in a variety of ways by different researchers, depending on the method of spike detection and separation used. We propose here a method of characterization that should provide a consistent basis for probe evaluation in these experiments. While these techniques are standard, the particular choices made will determine the methods to be used in the future in order to facilitate repeatability and side-by-side comparison. This method is then applied to the two site designs being evaluated in the current animal trials.

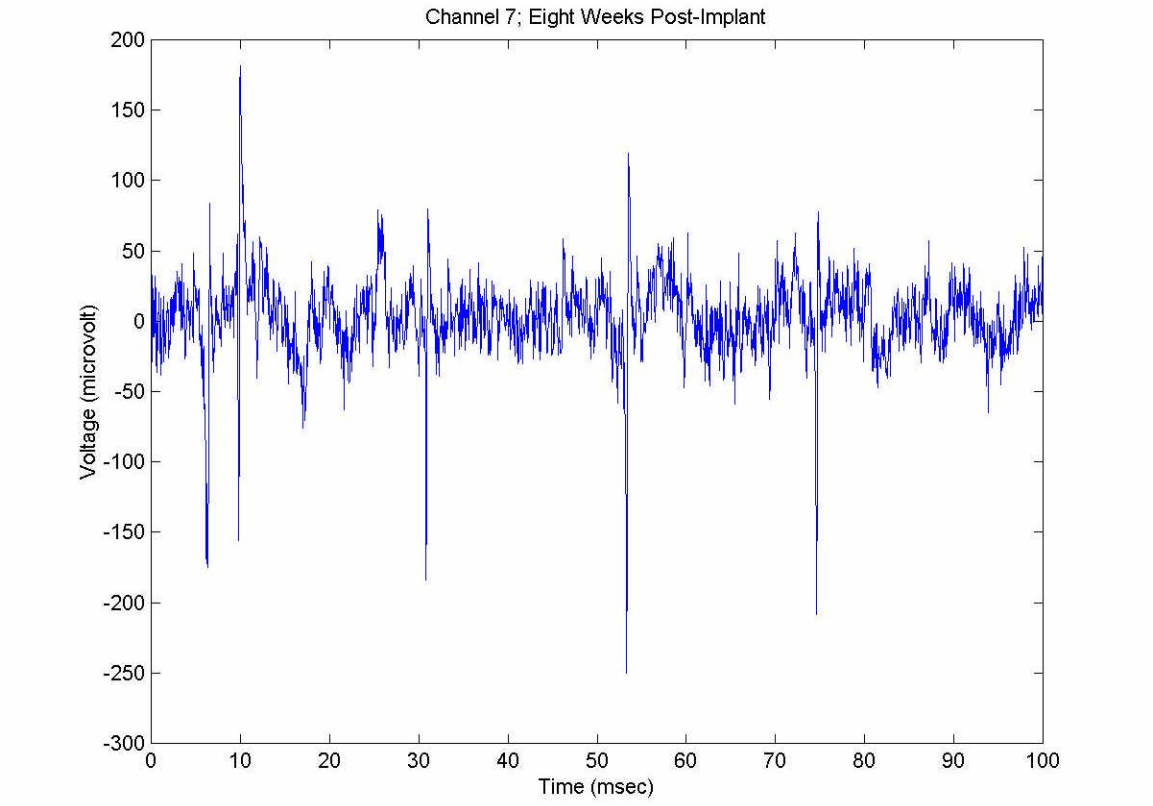


Fig. 6: Recording of driven neural activity in auditory cortex, eight weeks post-implant.

The probe recording characterization consists of an analysis of average spike waveforms and an analysis of noise. Each recording consists of a total of ten seconds of data per channel, recorded continuously and digitized at 20kHz. Recording is triggered by the presentation of a 50msec white noise burst, and recording continues for 50msec after the end of the stimulus. This 100msec sweep is repeated 100 times. In order to analyze the spike waveform, it is first necessary to extract action potentials from the neural record. This is accomplished by selecting negative-going spikes that exceed four standard deviations below the total signal average. This thresholding is accomplished in two stages, so that the spikes are first extracted based on the total standard deviation. The standard deviation is recalculated based on the remaining waveform, and the spikes are re-sorted based on the new ("noise") standard deviation. In this way, the contribution of spikes to the standard deviation is lessened. Next, a cluster plot is constructed using the first two principal components of the total separated spikes, and k-means clustering is used to separate the spikes into single units and eliminate spikes likely to have been caused by noise. Finally, a template (average) waveform is constructed for each separated single unit. The signal-to-noise ratio (SNR) is then defined as the peak-to-peak voltage of the template waveform to the standard deviation of the neural record with spikes extracted. Note that this is really a "single unit" SNR; if there is more than one unit extracted on a given recording channel, the channel SNR is defined as the greatest of the single unit SNR's. A comparison of SNR for each site type over the duration of the implant will indicate whether there is a significant advantage to one design. Eventually, the number of extracted spikes on a channel will fall to zero; the length of time for this to occur will be defined as the longevity of that site. Additional protocols involving the measure of stability using differences in template waveforms are being developed.

4.3 Initial Results from Silicon "Microwire" Implants

The purpose of the silicon "microwire" implants is to establish a baseline longevity and stability for chronic recordings with Michigan probes using our current best methods and to test the hypothesis that the degree of mechanical cleaning may affect the useful lifetime of a recording site. Our approach is to do a series of implants with these devices in order to compile a database of statistically independent single-unit recordings in the auditory cortex and then to characterize the overall success of the different site designs by using the measures described in the previous section and averaging over all of the observations. In this way, we hope to make sound design decisions despite the enormous variation in observed signal amplitudes found on a given electrode array.

The preliminary results given below are based only on the first implant. Because of the small number of sites (8 of each type) it will be necessary to gather more data before any conclusions can be reached. Note that the initial SNR's of the two site types are almost identical. After eight weeks, a difference in the SNR's has become apparent, with the tip sites being favored. However, a one-tailed t-test indicates that there is statistically significant difference only to 88% confidence. The data gathered from the second implant and from planned additional implants should help to settle this question.

	Implant Day One		*Implant Week Eight*	
	N	SNR	N	SNR
Tip Site	133	6.6	96	5.9
Standard Site	59	6.4	27	4.7

Table 1: Number of recorded spikes and Signal-to-Noise Ratio (SNR) for standard (center-mounted) and tip sites. The probe was implanted in guinea pig auditory cortex.

The rms noise on the two sites is almost identical, roughly 12μV initially, rising to nearly 18μV at week eight. It is interesting that the increase in rms noise scales pretty closely with the increase in real impedance observed in the signal bandwidth. As seen in Fig. 7, the impedance in our recording bandwidth of 100Hz to 3kHz rises on the order of 1 MΩ over eight weeks for the standard site; the result is similar for the tip site. Using $V_{noise}=(4kT\Delta f)^{1/2}$ we expect an increase of 7μV for this impedance rise.

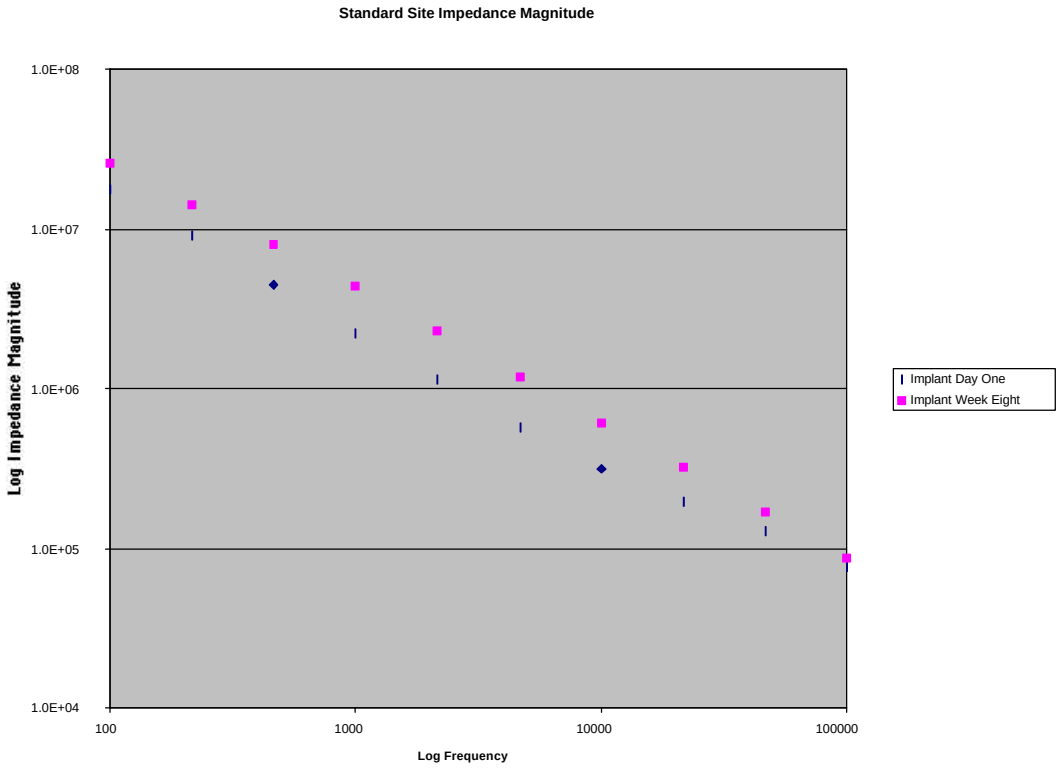


Fig. 7: Average impedance magnitude vs. frequency for a center-shank-mounted "standard" site on a chronic implant, initially and after eight weeks.

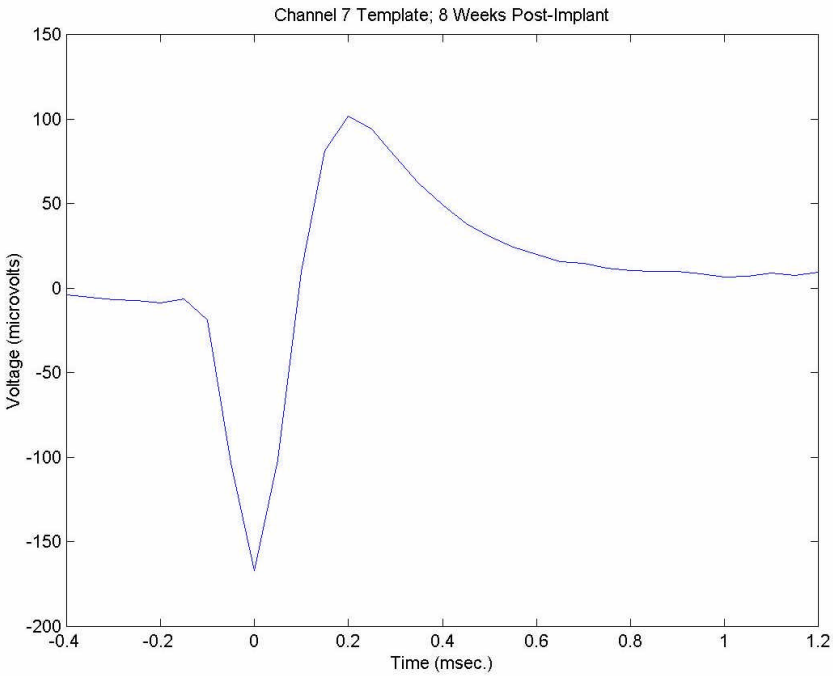


Fig. 8: Template (average spike waveform) for one channel of chronically implanted probe, eight weeks post-implant.

The larger site records a greater number of spikes, which seems to indicate that the activity is originating in more than one cell and that the difference is due to the increased recording area of the larger site. Yet, both the principal component analysis and an analysis based on the refractory period seen in the spike train autocorrelograms indicate that these are single units. Further analysis will have to be carried out to determine the cause of the difference in spike counts; in particular, there is a chronic probe that addresses this issue by varying the site overhang beyond the substrate with a constant site size.

Traces for one sweep on all sixteen channels are given below for one day (Fig. 9) and eight weeks (Fig. 10) post-implant. The increased noise on channel 5 was observed after approximately two weeks of implantation and was correlated with a rise in impedance at the same time. The site is not open, however, and is still recording spikes above the higher baseline noise level. We are hypothesizing that the increased noise is biological in nature, and we will try to correlate the difference with some change in histology when the animal is sacrificed.

5. Active Recording Probe Fabrication

During the past quarter, two active mask sets were designed. The mask sets include fifteen different probes, as well as test chips for the verification of new circuit designs. A summary of the probes is given below in Table 2. The active probes are

currently in fabrication. Work on these probes is expected to conclude in the coming quarter as they are tested in animals.

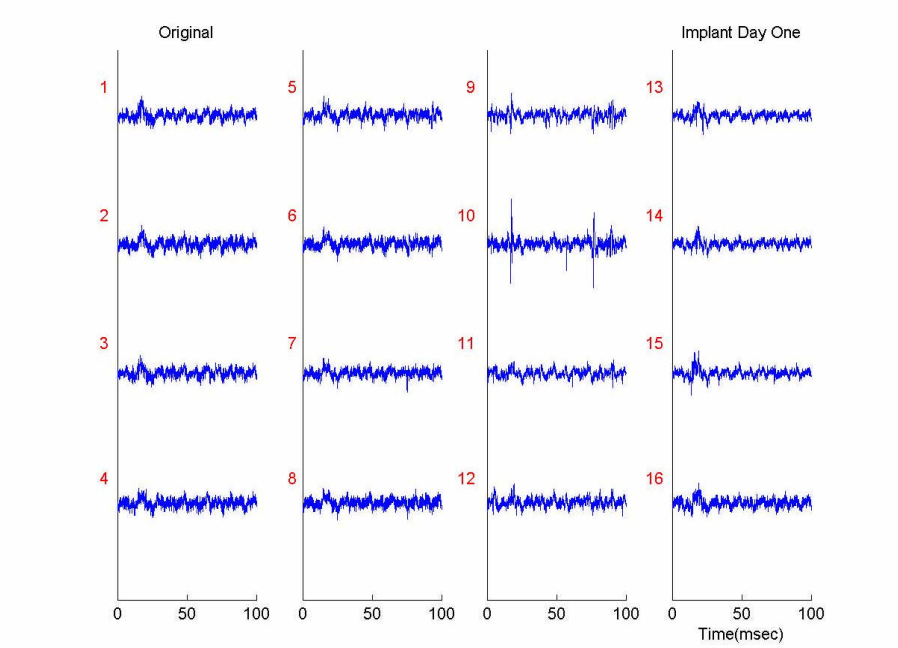


Fig. 9: Recording on the day of implantation in auditory cortex. Stimulus is a 50msec white noise burst. In this frame, large spikes are visible on channels 9 and 10, with somewhat smaller spikes on channels 7, 13 and 15. Evoked potentials are visible on most channels, centered at roughly 15msec.

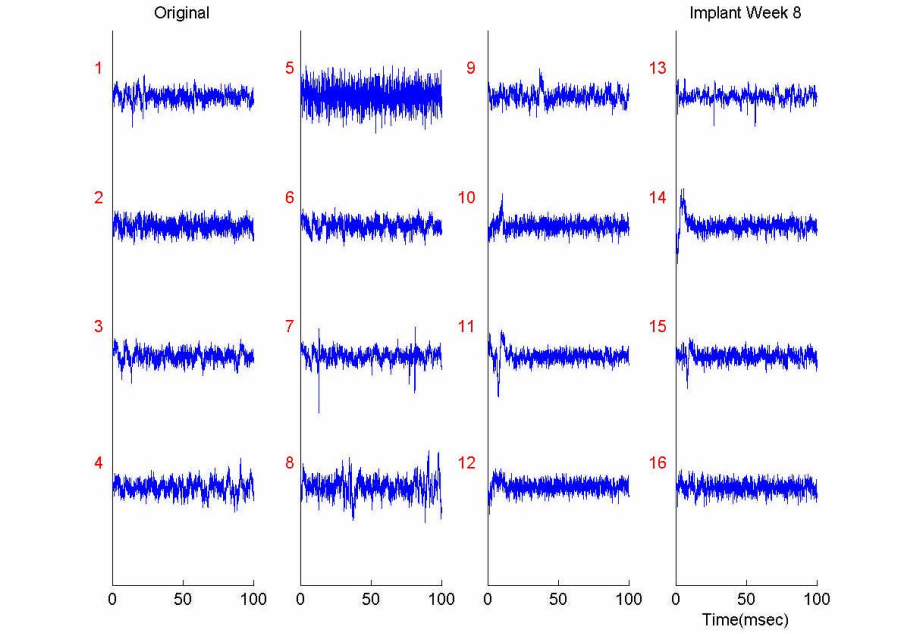


Fig. 10: Recording after eight weeks of implantation. Large spikes are visible on channels 7 and 8, with smaller spikes on channels 1,3,9, and 13. Evoked potentials are not as clearly evidenced in this frame, though they are routinely observed.

Probe Name	***Purpose***
PIA-2B	64 site front-end-selected, buffered probe
Phoenix1-3	64 site front-end-selected probes with improved buffers/amplifiers and DC stabilization
DC1-4	small probes for comparing DC stabilization techniques
Probe_2_2_1 Probe_4_4_1 Probe_4_4_2	four-shank four-site probes with newly designed closed-loop amplifiers in different feedback configurations
Buzsaki96	96 site buffered probe
Buzsaki64	64 site buffered probe
Phoenix_chronic	front-end-selected probe for chronic implantation
Passage	front-end-selected probe with closely-spaced sites for demonstration of "electronic passage."

Table 2: Active probe designs on new mask sets.

6. Readout Circuitry for Active Recording Probes

During the past quarter, four new active probes have been laid out and are currently being fabricated. These probes feature new electronics, including several amplifiers and a time-division multiplexer. All of the electronics have been designed for minimum power and area while still meeting the performance specifications required for this application. In addition, special care has been taken to ensure the operation of the circuits over the wide range of process variations typically found in our laboratory. The first probe is a four-shank four-site probe with an amplifier for each recording site. A transistor level schematic of the amplifier used on this probe can be seen in Fig. 11. The amplifier's feedback configuration is shown in Fig. 12.

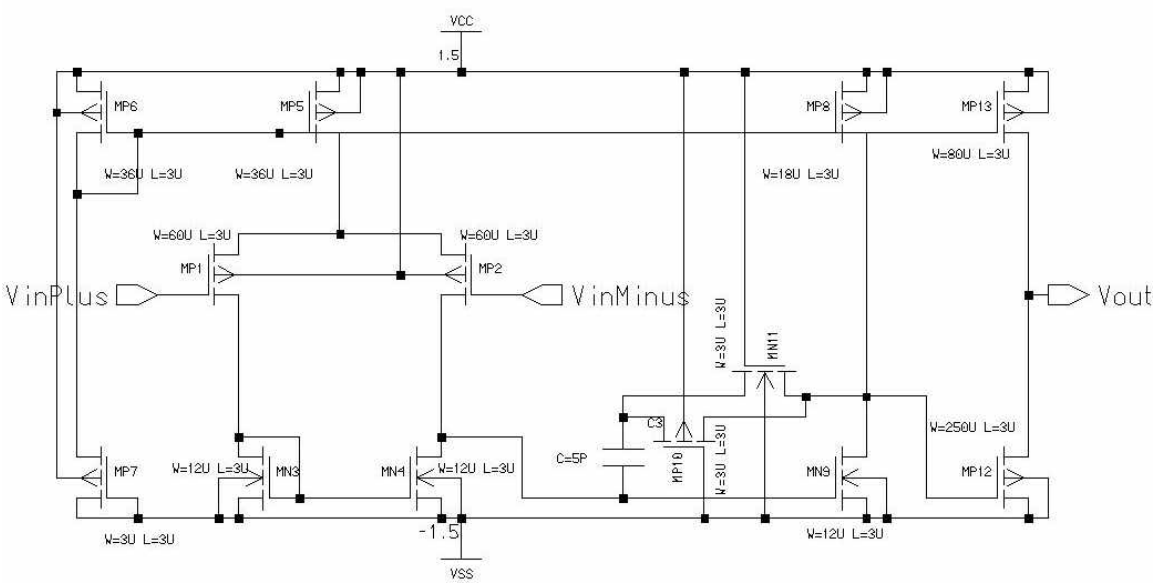


Fig. 11: Amp1 Buffered

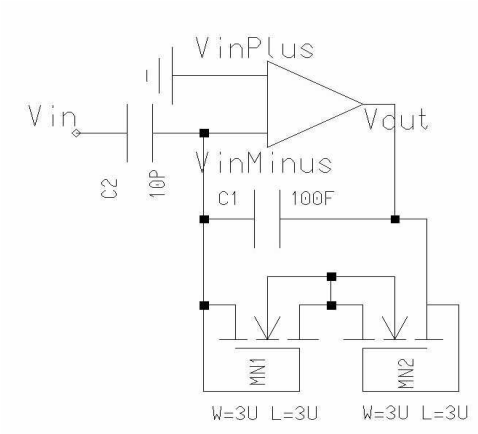


Fig. 12: Amp4 Buffered

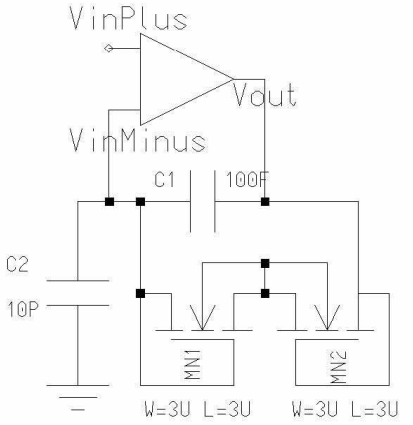


Fig. 13: Amp2 Buffered

Amp1 buffered is a standard two-stage op amp with a source follower at the output. Transistors M10 and M11 as well as capacitor, C, are used to compensate the amplifier and to set the upper cutoff frequency. The feedback applied in Fig. 12 is used to set both the in-band gain, C2/C1, and the lower cutoff frequency determined by C1 and the sub-threshold impedance of diode-connected transistors M1 and M2. Furthermore, this feedback configuration provides a DC gain of zero, allowing the amplifier to operate at any DC baseline potential. This amplifier has been laid out and thoroughly simulated after extracting parasitic capacitances. The AC response of the amplifier can be seen in Fig. 14, and a table summarizing its characteristics is presented below.

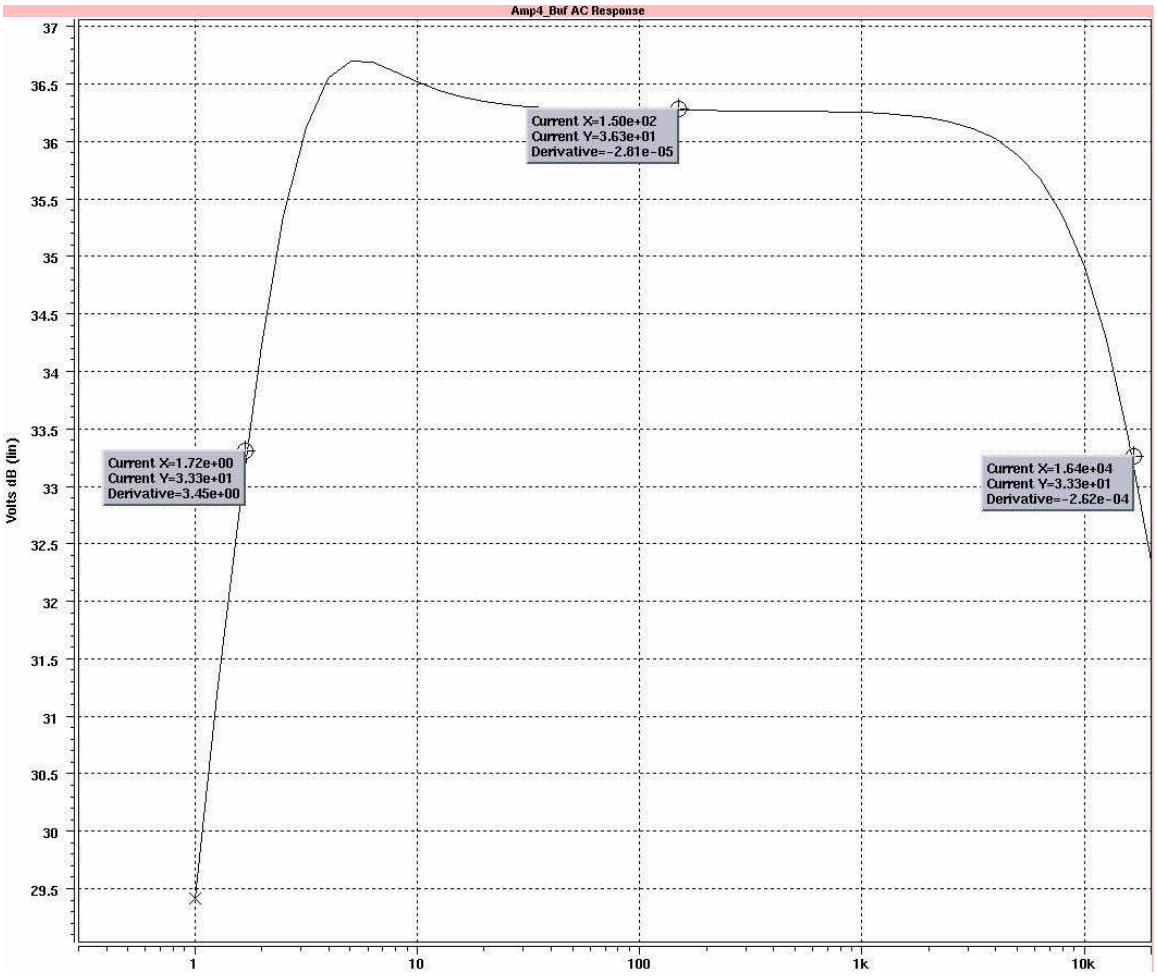


Fig. 14: Amp4 Buffered AC response

Gain	36.3db
Bandwidth	1.7Hz to 16kHz
Power Consumption	96.5μW
Input Referred Noise	6.4μVrms/√Hz
Layout Area	0.078mm^2

Table 3: Amp4 Buffered specifications

The second probe developed is also a four-site four-shank probe with an amplifier for each recording channel. The same amplifier is used but it is now connected in the feedback configuration shown in Fig. 14 above. This amplifier is less susceptible to gain loss due to parasitic capacitances and has a lower input-referred noise than Amp4 Buffered. This amplifier, however, has a DC gain of unity, limiting the amount of DC

baseline suppression. The in-band gain of the amp is 1+C1/C2, and the lower cutoff frequency is again determined by C1 and transistors M1 and M2. The amplifier has been laid out and simulated with parasitic capacitances extracted. The amplifier will operate over the typical DC baseline range of ±300mV. The AC response of the amplifier can be seen in Fig. 15; a table summarizing the performance characteristics is given below.

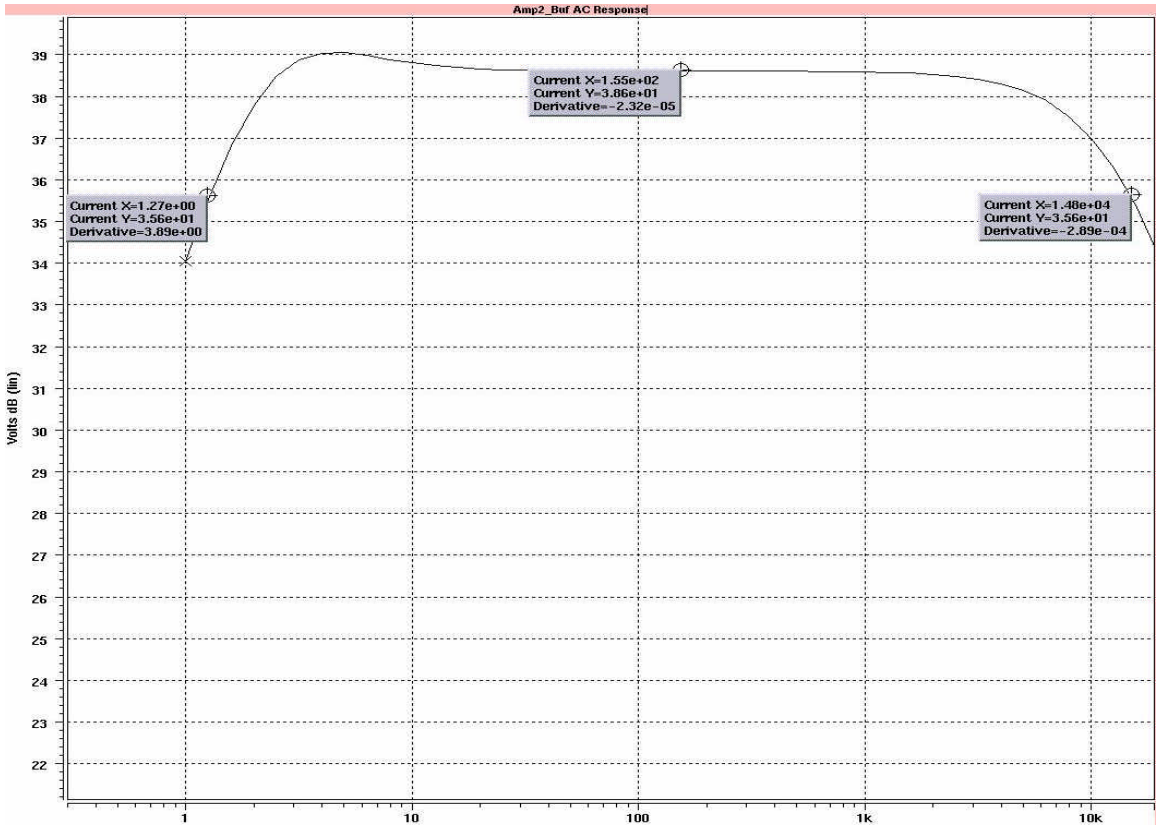


Fig. 15: Amp2 Buffered AC response

Gain	38.6db
Bandwidth	1.3Hz to 15kHz
Power Consumption	95.5µW
Input Referred Noise	5.4µVrms/√Hz
Layout Area	0.086mm^2

Table 4: Amp2 Buffered specifications

The third probe currently in fabrication is a two-site two-shank probe with two amplifiers per channel. The first of the two amplifiers, Amp3, is the unbuffered amplifier shown in Fig. 16 connected in the feedback configuration shown in Fig. 12. The AC response of this amplifier is displayed in Fig. 17, and a table listing its specifications is given below. The second amplifier is the same as that shown in Figs. 11 and 13 and is

discussed in detail above. Together the amplifiers provide a gain of ten thousand while consuming very little power or area.

Gain	36.7db
Bandwidth	2Hz to 17KHz
Power Consumption	49μW
Input Referred Noise	6.4μVrms/√Hz
Layout Area	.058mm^2

Table 5: Amp3 Unbuffered specifications

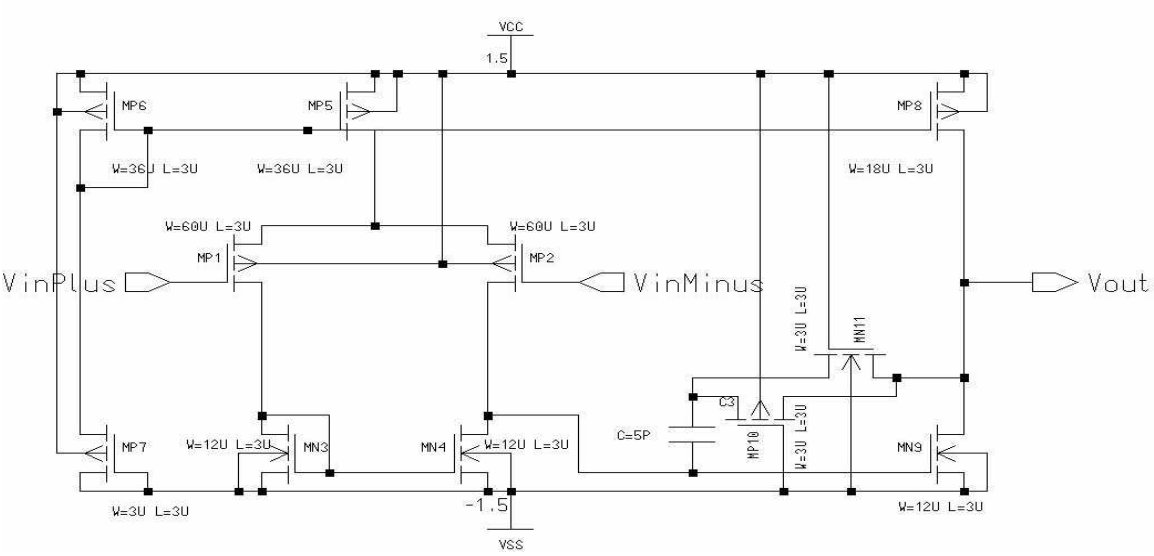


Fig. 16: Amp3 Unbuffered

The fourth and final probe being fabricated is an eight-site two-shank amplified and time-division-multiplexed probe. A system-level block diagram of the probe is shown below. The probe features eight Amp4 Buffered pre-amplifiers that were discussed above, a counter-decoder time-division multiplexer, and an additional amplifier to add gain to the desired signal and attenuate clock feed-through. A diagram of the time division multiplexer is presented in Fig. 19. A three-bit counter cycles through all of the eight sites and repeats this until a logic low is seen on the reset line. When the reset signal returns to a logic high, the multiplexer begins cycling through the sites again starting with site zero.

The counter consists of two inverters and two T-registers. The counter makes use of both the falling and rising edges of the clock to prevent clock transitions in the middle of the sampling window and to reduce the required clock frequency. Furthermore, the buffered clock signal is used as an output of the counter to save power and area. For this

reason, a 50% duty cycle clock should always be used with this design. The counter consumes an area of 0.062mm^2 while the decoder has a layout area equal to 0.041mm^2. A transistor level schematic of the T-register is shown in Fig. 20.

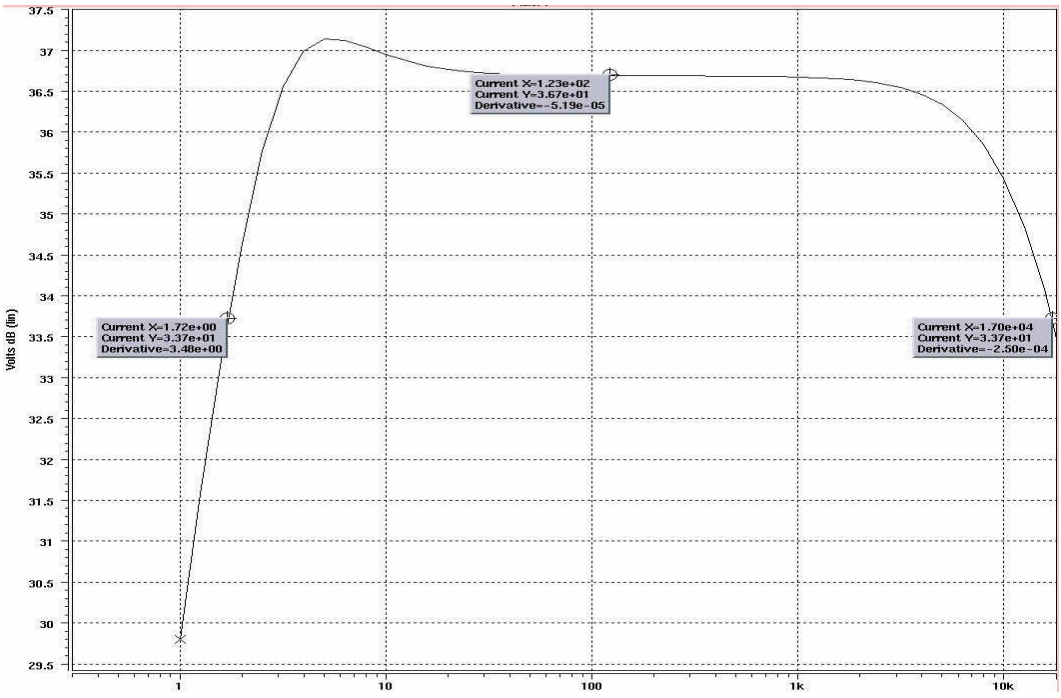


Fig. 17: Amp3 Unbuffered AC response

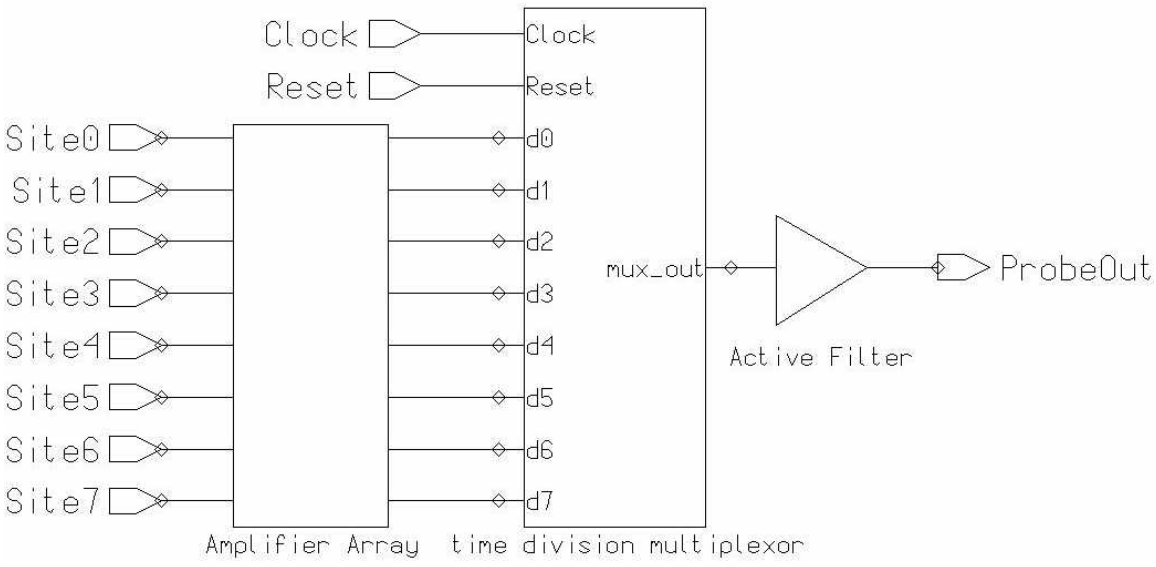


Fig. 18: System-level block diagram of the multiplexed probe

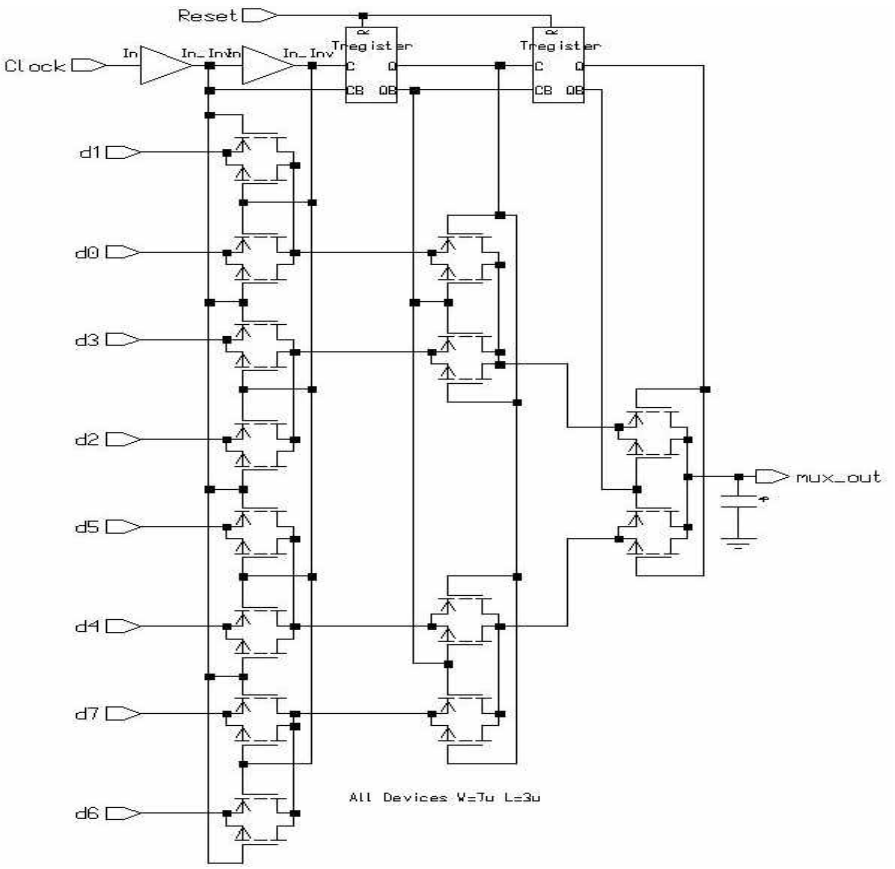


Fig. 19: Time-division multiplexer

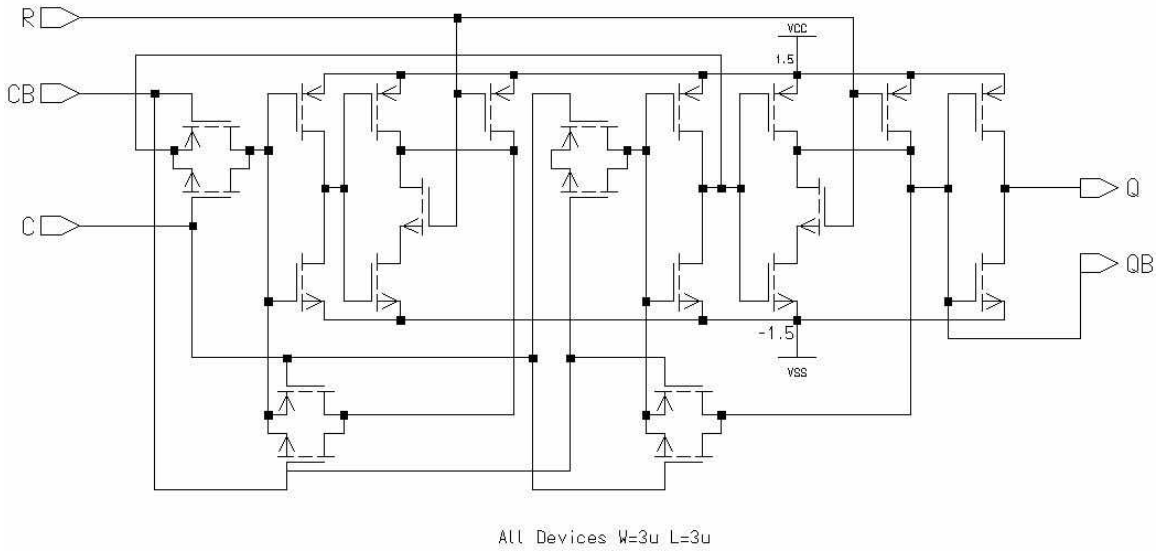


Fig. 20: T-Register schematic

At the output of the multiplexer, clock feed-through appears as 20nsec pulses at the end of the sampling interval. The amplitude of these pulses is comparable to that of the neural signals. Since this is undesirable, an amplifier has been used to filter the clock feed-through while providing some extra gain to the neural responses. The feedback shown in Fig. 21 was applied to Amp1 Buffered to suppress the clock feed-through. The AC response of this amplifier is shown in Fig. 22, and it can be seen that the amplifier should provide a gain of 10 to the neural signals while eliminating the undesired 20nsec pulses. Table 6 lists the specifications of the active filter.

After the entire probe was laid out, the electronics were simulated with pulses of different amplitudes, pulse widths, and pulse delays applied to the eight pre-amplifier inputs. A clock frequency of 50kHz was also applied. A transient analysis was performed and is displayed in Fig. 23. It can be seen in Fig. 23 that the clock pulses do, in fact, occur at the end of the sampling interval and that their amplitude as been attenuated to a value well below that of the amplified neural signals.

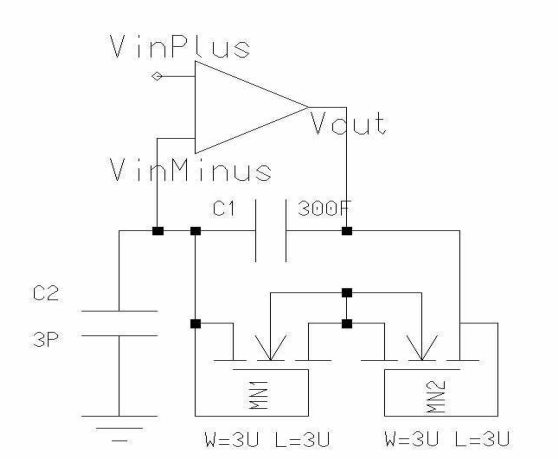


Fig. 21: Active filter schematic

Due to the large power supply swings possible in telemetry applications, a special amplifier with increased power supply rejection has also been developed. The amplifier uses a fully differential folded cascode architecture and a kT/q voltage reference to achieve its power-supply independence. A block diagram of the amplifier is shown in Fig. 24.

The differential feedback is the same as that applied to Amp4 Buffered with the in-band gain per stage set by the capacitor ratio C1/C2 and the low frequency cutoff set by the feedback capacitor and the feedback transistors. The gain of the first stage is set here to 100 while the gain of the second stage is set to 22. The two amplifiers that comprise the telemetry amplifier system are slightly different, and a transistor level schematic of the unbuffered folded cascode is pictured in Fig. 25, with its common mode feedback circuit shown separately in Fig. 26.

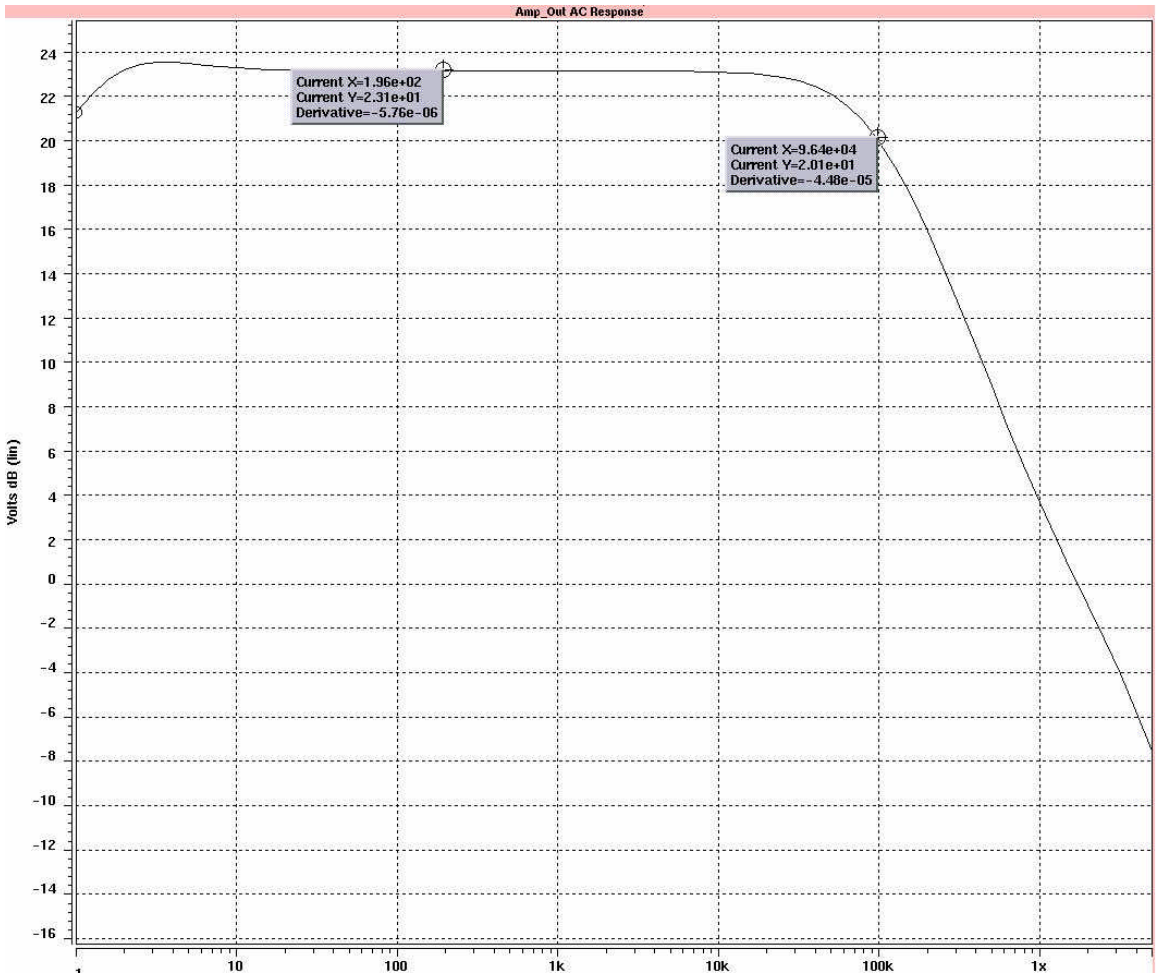


Fig. 22: Active filter AC response

Gain	23.1db
Bandwidth	<97KHz
Power Consumption	96.5µW
Input Referred Noise	10.2µVrms/√Hz
Layout Area	.068mm^2

Table 6: Active filter specifications

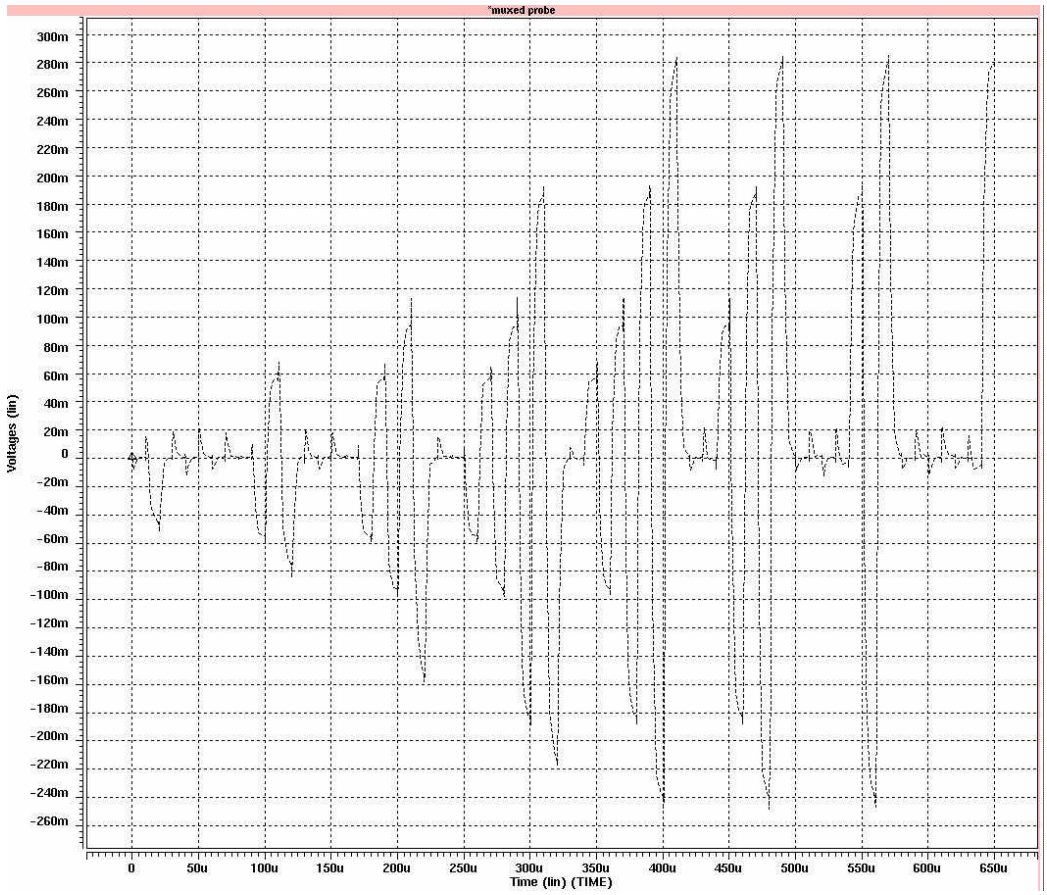


Fig. 23: Multiplexed probe transient response

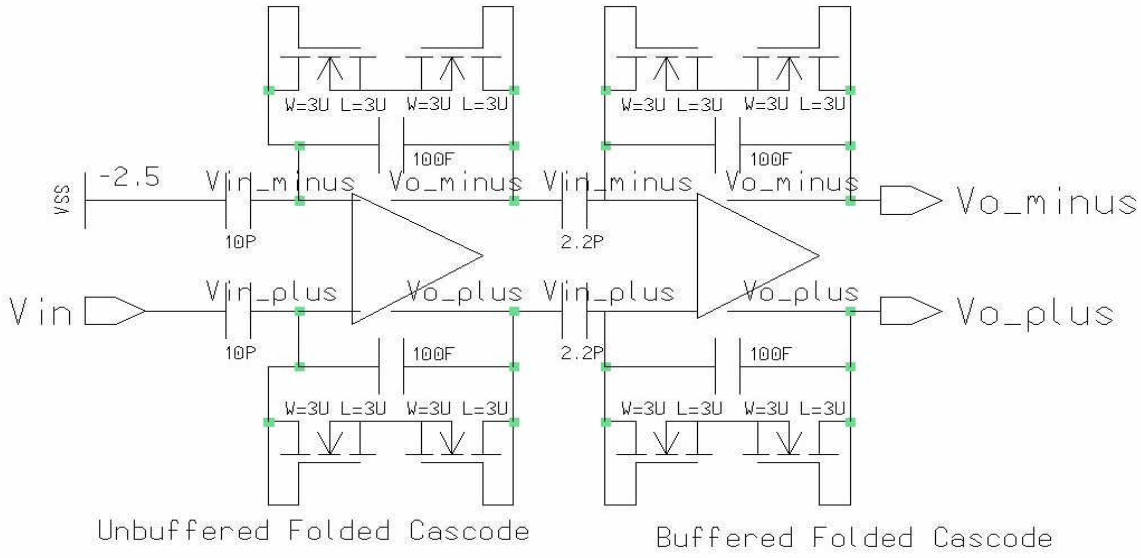


Fig. 24: Telemetry amplifier diagram

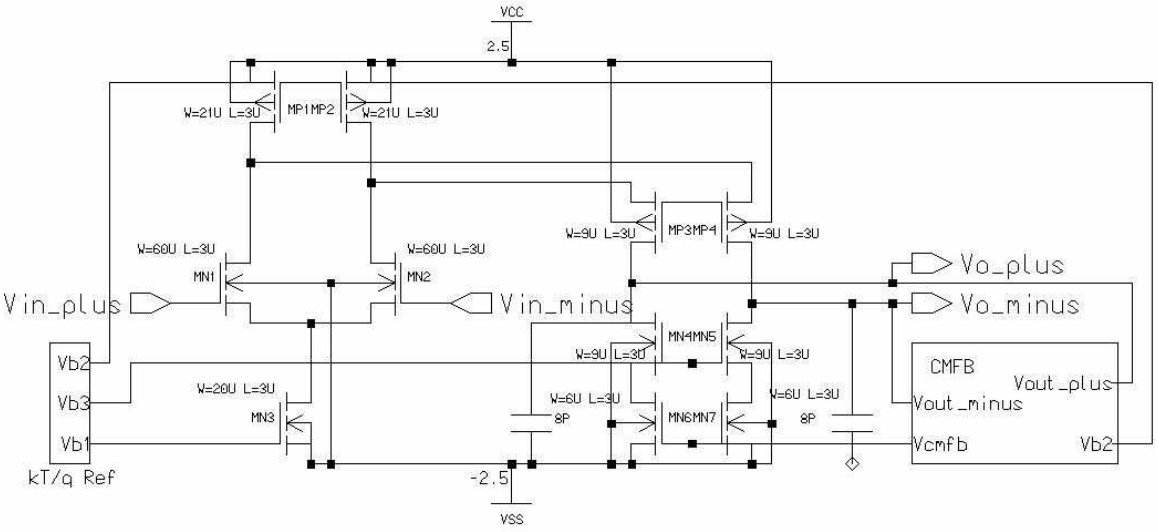
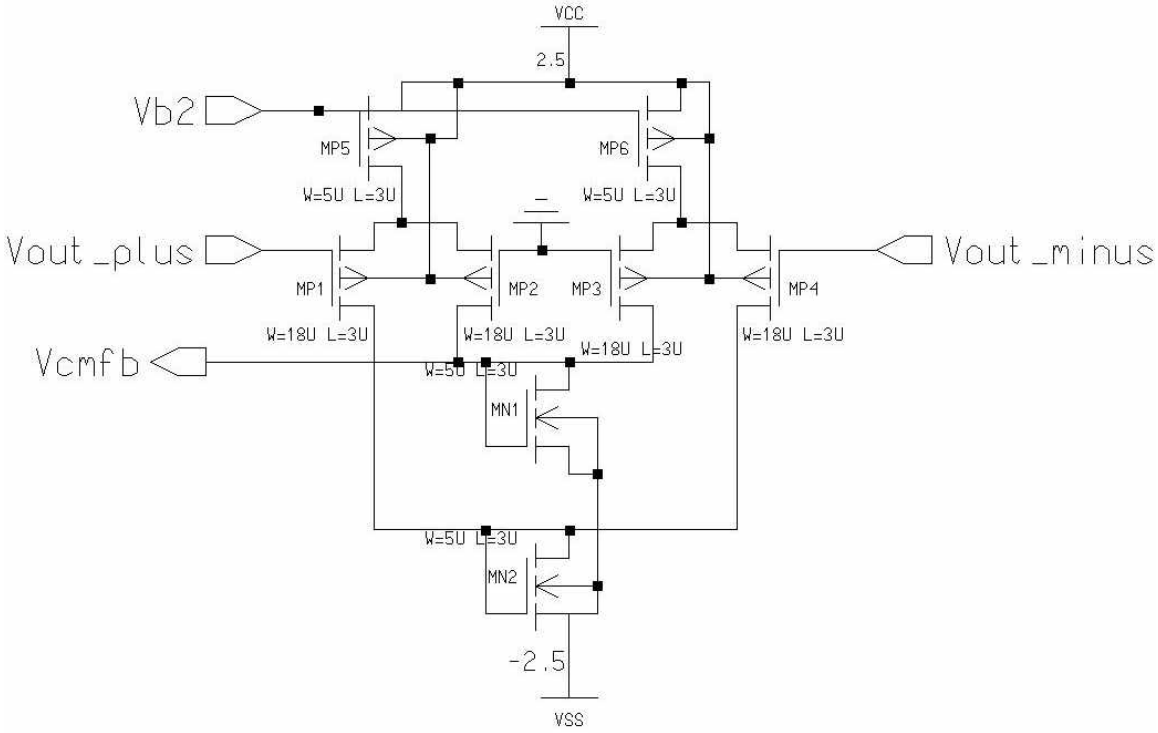


Fig. 25: Unbuffered folded cascode circuit.

Fig. 26: Common-mode feedback for the unbuffered folded cascode.



The amplifier shown in Fig. 25 is not buffered because it only has to drive a very high impedance node and the elimination of the buffers saves both power and area. The upper cutoff frequency of the amplifier is set by the two load capacitors and the common mode output voltage is set to ground by the common mode feedback circuit. The unbuffered folded cascode has been laid out along with its common mode feedback circuit and together they consume an area of only $0.098mm^2$.

The buffered folded cascode is shown in Fig. 27, with its common mode feedback circuit shown in Fig. 28. The requirements on this amplifier are more stringent than that of the unbuffered version since it must be able to drive either a bond pad or a ribbon cable connection. Furthermore, the common mode feedback must be designed to remain linear over the output voltage swings from ±500mV, a nontrivial achievement. For these reasons the buffered cascode consumes more power (219μW) than its unbuffered counterpart (80μW). The upper cutoff frequency of the amplifier is again determined by the 8pF capacitors and the common mode output voltage is centered around ground.

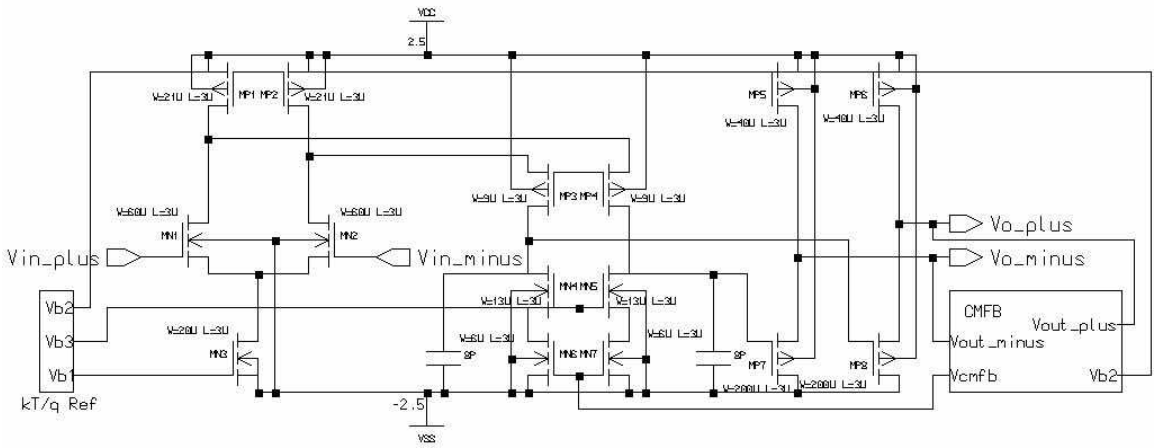


Fig. 27: Buffered folded cascode

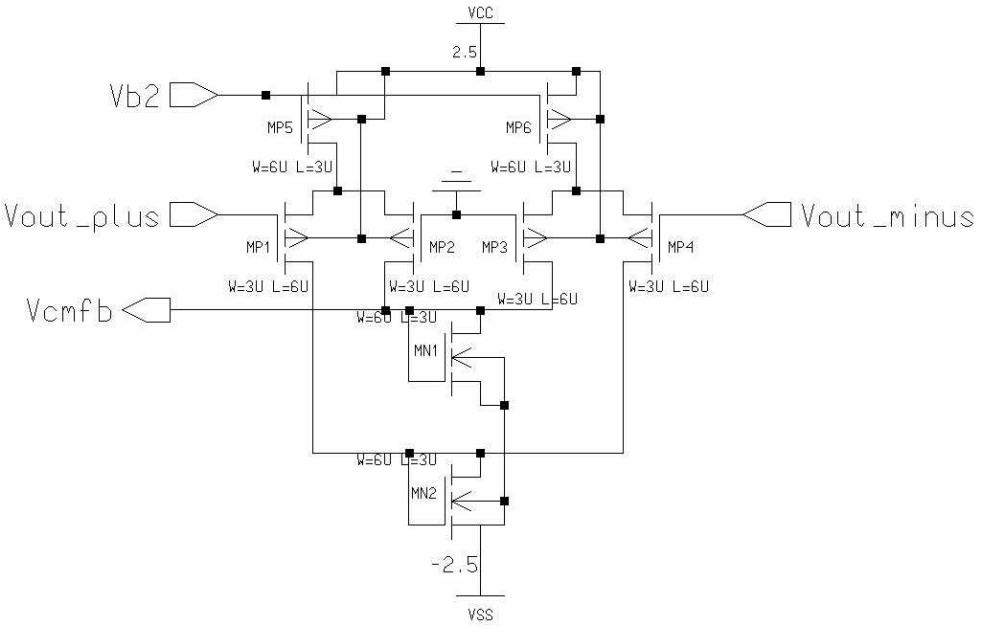


Fig. 28: Common mode feedback for the buffered folded cascode

Both of the amplifiers are biased from the same kT/q reference. This type of reference is used to both increase the power supply rejection of the amplifiers and to reduce the amount of output common mode voltage shift associated with varying transistor thresholds. The kT/q reference has been laid out and it consumes a total area of $0.028mm^2$. A transistor level schematic of the reference is shown below in Fig. 29.

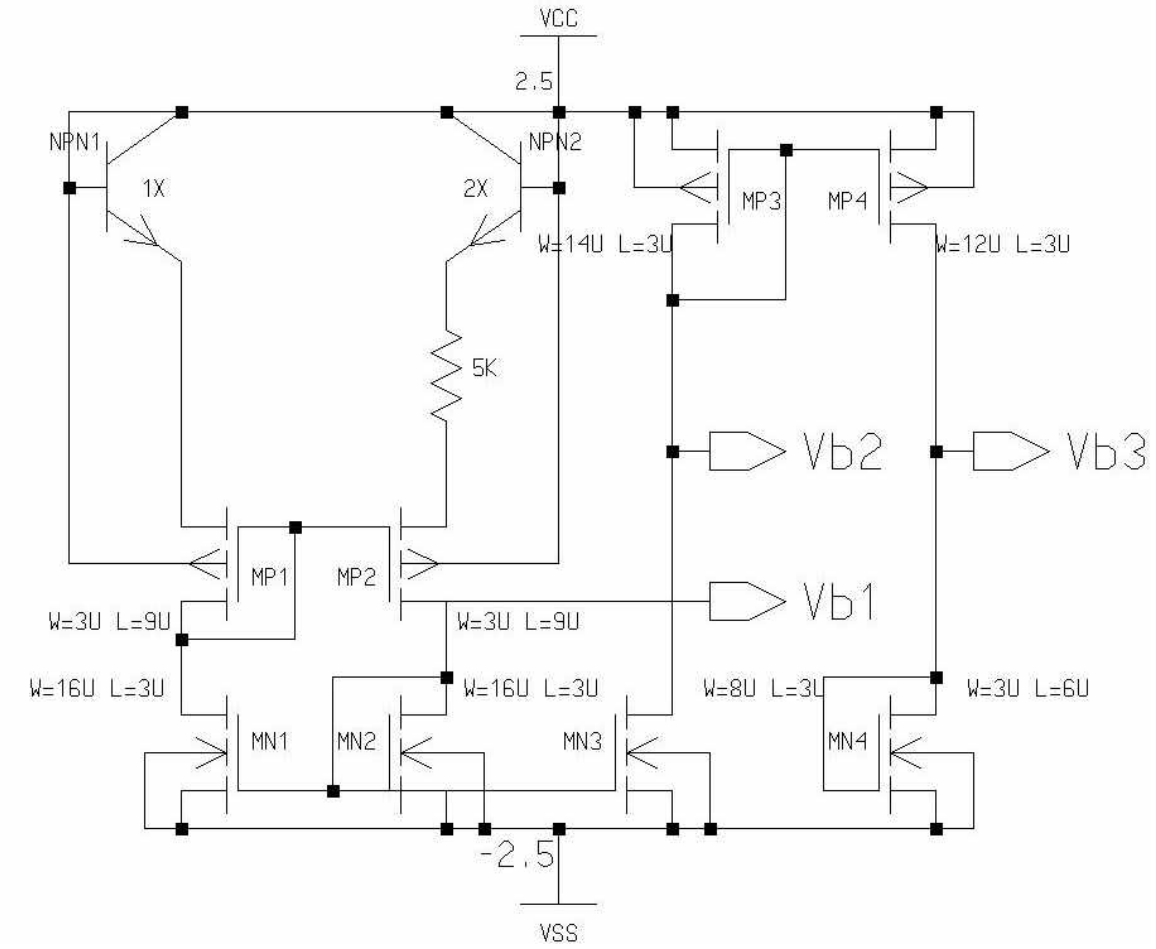


Fig. 29: kT/q reference

The telemetry amplifier has not been fully laid out but it has been thoroughly simulated. The AC response of the amplifier is shown in Fig. 30. Since the carrier frequency of the telemetric link is 4MHz, the telemetry amplifier was tested to determine its ability to reject 4MHz supply ripple. To do this a transient analysis was performed with a 60μV, 100μsec pulse present at the input of the amplifier while a 100mV ripple at 4MHz was placed on the positive supply. It can be seen in Fig. 31 that the supply barely even couples into one of the single ended outputs. Furthermore, when the output is taken differentially, the power supply ripple cannot even be detected in the output signal. This near perfect performance will obviously not be achievable, but with special care taken to make the amplifier symmetrical during layout, very good performance should be achieved.

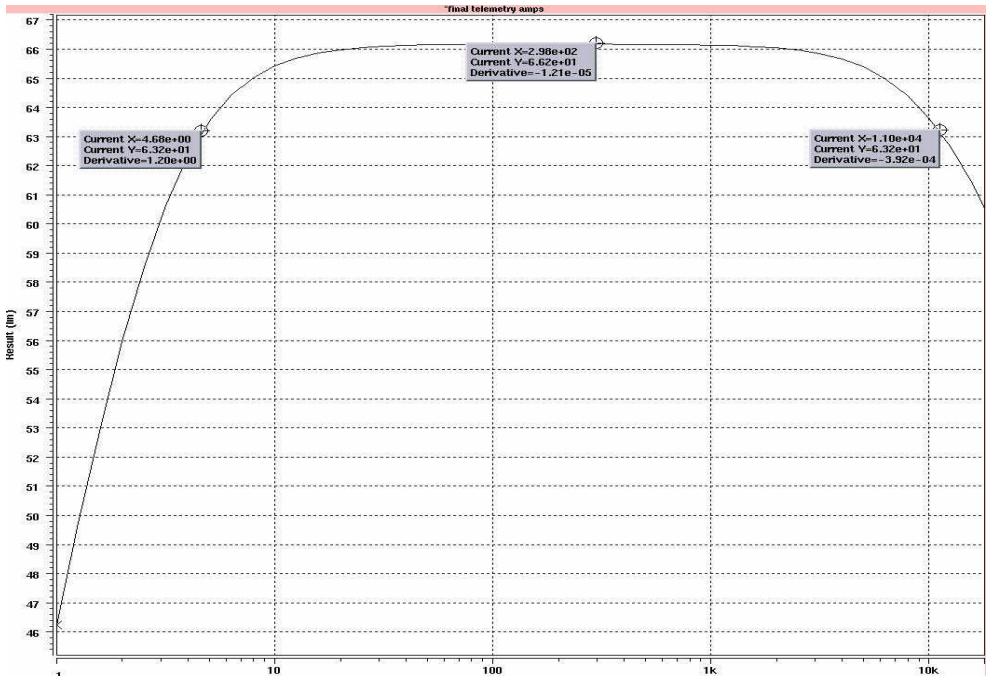


Fig. 30: Telemetry Amplifier AC Response

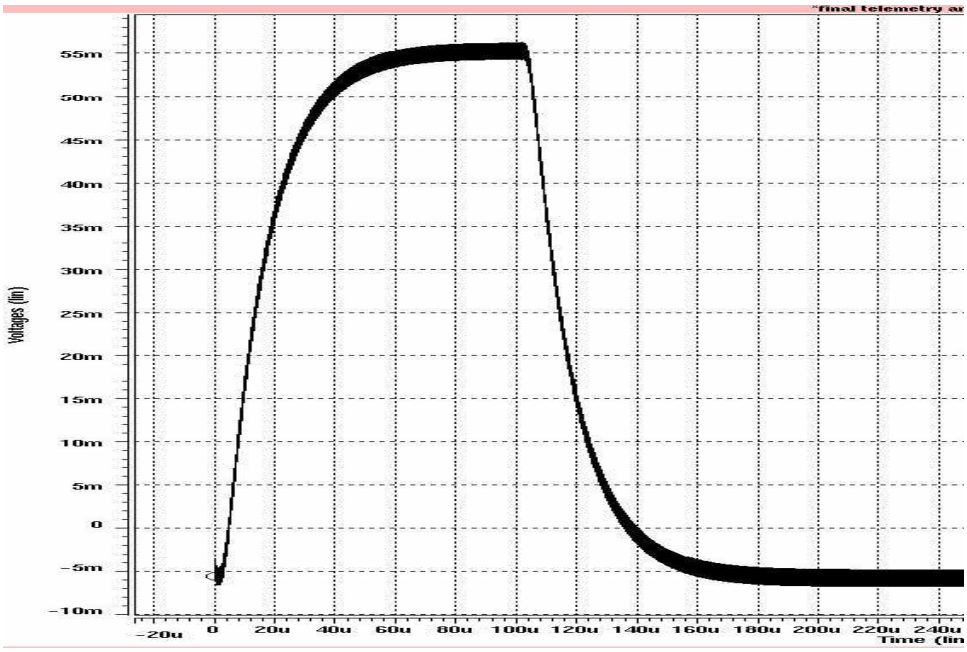


Fig. 31: Single-ended transient response to a 60µV pulse with 100mV of 4MHz supply ripple

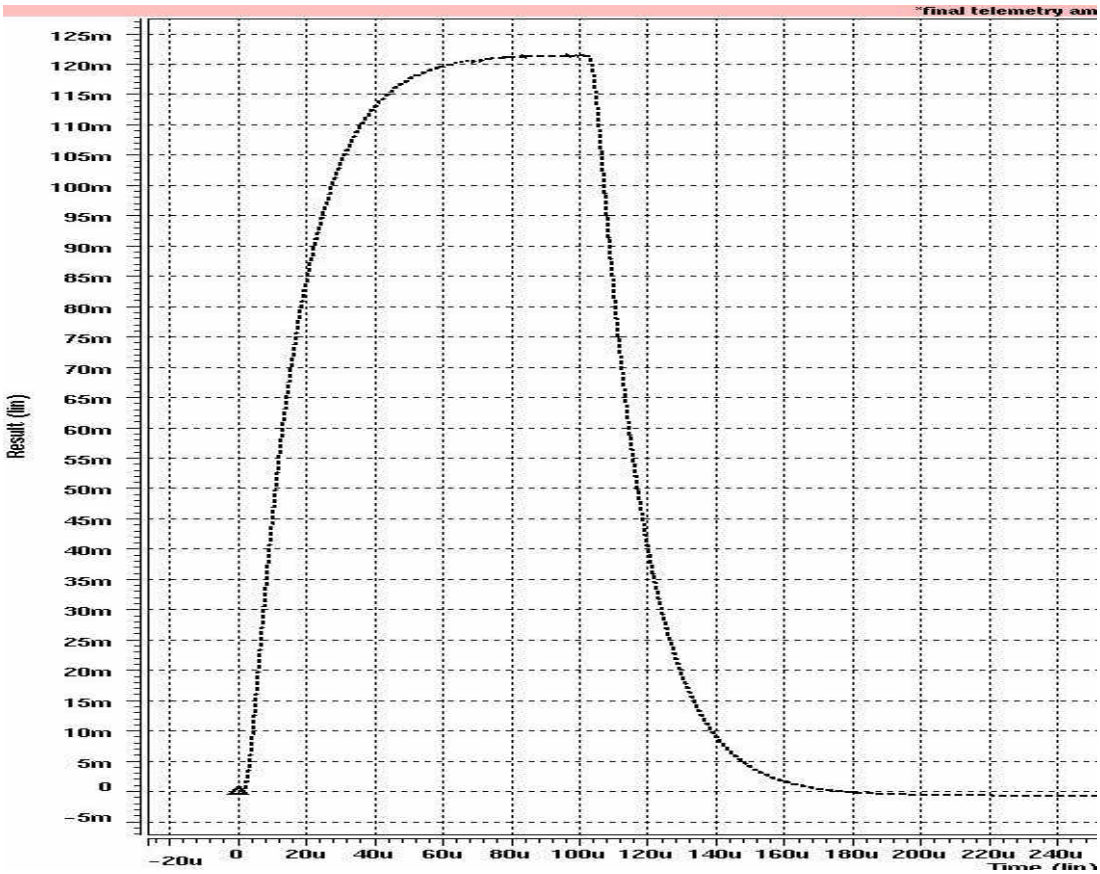


Fig. 32: Differential transient response to a 60μV pulse with 100mV of 4MHz supply ripple

Gain	66.2db
Bandwidth	47Hz to 11KHz
Power Consumption	423μW
Input Referred Noise	5.7μVrms/√Hz

Table 7: Telemetry amplifier specifications

7. Test Results Circuit Blocks For A Wireless Recording System

In the last progress report we reported that the circuit chips containing a number of circuit blocks to be used in a wireless recording system had been received from MOSIS and were undergoing test and characterization. During the last quarter, testing of this chip was completed and modifications were made to improve circuit performance. These tests are described below.

Figure 33 shows the overall block diagram of the circuits that were included on this chip. The chip includes circuit blocks for voltage regulation, envelope detection, and clock recovery. It should be noted that these circuit blocks are different than previous circuits designed by our group for implanted telemetry systems used in stimulating systems. The main difference is that circuits used in the recording system have been designed using an all-CMOS foundry-compatible technology, instead of the in-house BiCMOS process we have used for stimulating system. The motivation for using an all-CMOS technology is to utilize the higher density that a foundry process offers since it uses a device feature of as small as 1.2µm. This smaller feature size allows us to pack more devices into a smaller area and to take advantage of future smaller feature sizes that are offered through the foundry.

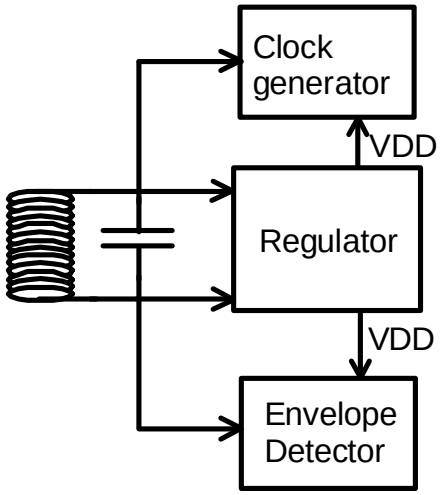


Fig. 33: Block diagram of the circuits included in the fabricated chip.

Device Level Tests

The first set of tests were conducted to measure the threshold voltage of transistors produced by the foundry process. In designing these circuit blocks, the threshold voltage values that were provided by the foundry were expected to be in the rangesof 0.5-0.7V for NMOS and 0.6-0.9V for PMOS transistors. After receiving the chips and measuring the threshold voltage of the transistors, we found that the threshold voltage for pMOS transistors was actually -1.06V. This is much higher than expected, and has caused a number of the circuit blocks not to function properly. After this observation, we checked the threshold voltages of a number of chips fabricated through MOSIS AMI 1.2µm process. These are listed in Table 8. As is evident, the threshold voltage of NMOS transistors varies from 0.59V to 0.7V, while the threshold voltage of PMOS varies from -0.75v to –0.97v. This shows that the PMOS threshold voltage presents more variation than NMOS, so we need to pay more attention during design and simulation to making sure that the circuits are functional in the presence of such large variations. One way to do this is to use more NMOS transistors rather than PMOS transistors in circuit design for better and more consistent circuit performance.

Table 8: Threshold voltage of transistors fabraicated in the AMI ABN 1.2μm process

Run Number	1	2	3	4	5	6
Vth (NMOS)	0.6897	0.6222	0.6548	0.6413	0.6401	0.6897
Vth (PMOS)	-0.7674	-0.7654	-0.9683	-0.9604	-0.8061	-0.7574
Run Number	7	8	9	10	11	
Vth (NMOS)	0.6622	0.6315	0.6063	0.5940	0.6041	
Vth (PMOS)	-0.7878	-0.7989	-0.9084	-0.8135	-0.8583	

Based on the statistics of the threshold voltages of the chip we received, which was fabricated using the AMI ABN 1.5μm process, we have determined that we should use the following threshold voltage values for the two transistors: 0.65V ± 9% for NMOS threshold voltage and 0.9V ± 15% for PMOS threshold voltage.

In spite of this large discrepancy between the expected threshold voltage values, and the actual measured values, the front-end chips were extensively tested in the last two months. Some of the testing results are described below.

Voltage Regulator:

The voltage regulator is one of the most important circuit blocks in the entire system because it has to provide a stable and low-noise voltage and consume a small amount of power. Figure 34 shows the block diagram of the regulator. It consists of a bandgap voltage reference which generates the stable voltage level, an amplifier that together with resistors in its feedback loop generates the 5V supply needed, and a startup circuit that will ensure that the regulator will not lock to 0V. The entire voltage regulator circuit has been tested and as expected it does not operate properly because of the large shift in the threshold voltage of the pMOS transistor. Therefore, we have had to test the individual blocks in the regulator. One of these is the bandgap reference.

The measurement results of bandgap reference circuitry are listed in Table 9, which also shows the measured power dissipation of the entire chip. The bandgap reference block is fully functional in spite of the shift in the pMOS threshold voltage. The measurement result of V_{ref} matches the expectation.

The amplifier circuit block did not operate properly because of the shift in pMOS threshold voltage. The effect of the threshold voltage shift on the amplifier has been simulated. The simulation results of the prototype amplifier are shown in Fig. 35. For normal threshold voltage, the unity-gain frequency is higher than 10MHz as designed, and phase margin is about 80°, as shown in the upper graph in Fig. 35. However, for large PMOS threshold voltage, the unity gain frequency of the amplifier is moved toward lower frequency, where it is much less than 4MHz, the carrier frequency of the telemetry

link. A unity gain frequency of 100kHz is observed in this case, as shown in the lower gragh in Fig. 35. We also note that the cut-off frequency of the amplifier is much lower in the case of large PMOS threshold voltage.

The same comparison is also made for the amplifier when the feedback is applied. In our simulation, the feedback is designed to obtain a gain of 6dB for low frequency signals; the simulation result is shown in Fig. 36.

Table 9: Measured results of V_{ref} and power consumption

Chip	Bandgap Reference voltage Vref (V)	I_{DD} (mA) VDD=5v	Power Consumption (mW)
#1	1.426	0.686	3.43
#2	1.419	0.715	3.58
Expected	1.423 (Hspice)	0.9	4.5 (Hspice)

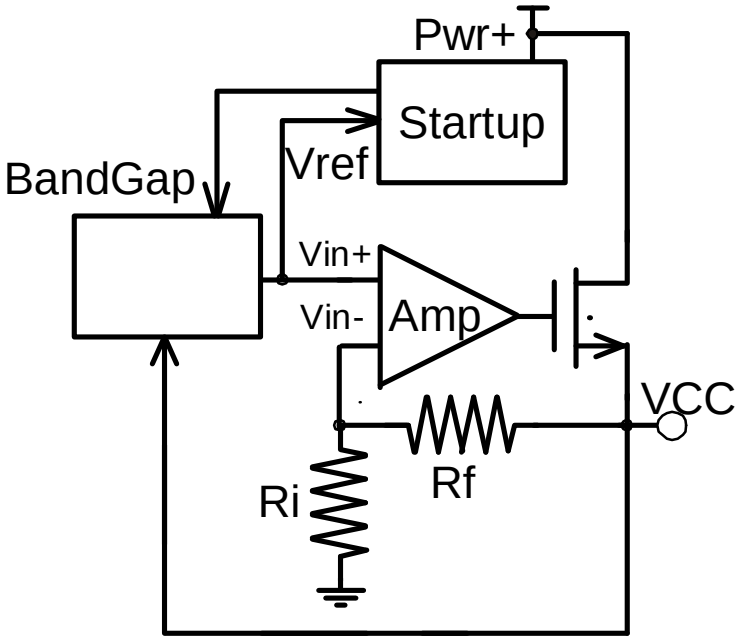


Fig. 34: The schematic of voltage regulator

At low frequency, under 100kHz, the overall gains are the same in two cases no matter what the threshold voltages are. However, the circuit with the normal threshold voltage works well at 4MHz, but the overall gain is only –18dB if the PMOS threshold voltage shifts higher to 1.0V. In other words, if the PMOS threshold voltage shifts too much, the amplifier cannot accomplish the function of amplifying signals with a frequency of 4MHz or above. The amplifier has been redesigned to be capable of operation in spite of large shifts in the threshold voltage of transistors.

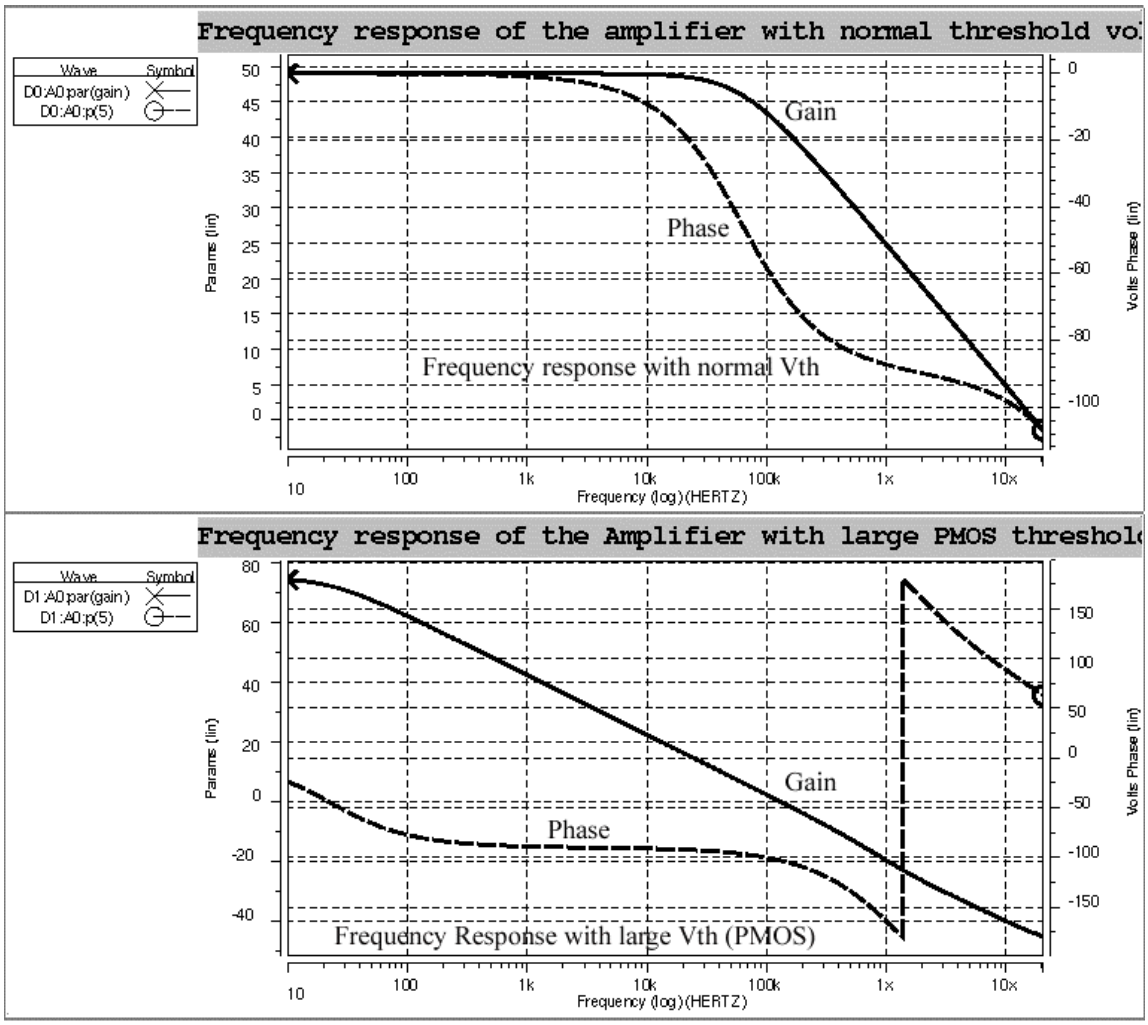


Fig. 35. The frequency response of the amplifer.

Clock Recovery Circuitry:

The clock generating circuitry recovers the 4 MHz square wave signal for the on-chip clock from the sinusoidal signal received by the on chip coil. The input and output waveform of the clock recovery circuitry is shown in Fig. 37. The clock generating circuitry works as designed.

Envelope Detector

The envelope detector is composed of a band-pass filter (BPF) followed by a Schmitt trigger. We have simulated the frequency response of the BPF with the large shift in PMOS threshold voltage with the results shown in Fig. 38. Originally, the gain of the BPF was designed to be 7dB for a 20kHz signal. However, the gain is changed to –20dB if the PMOS threshold voltage is shifted to –1.06V. We also note there is no obvious lower cut-off frequency for the BPF. As the result, this block failed to pick up the 20kHz signal from 4MHz carrier, and we have not been able to test it.

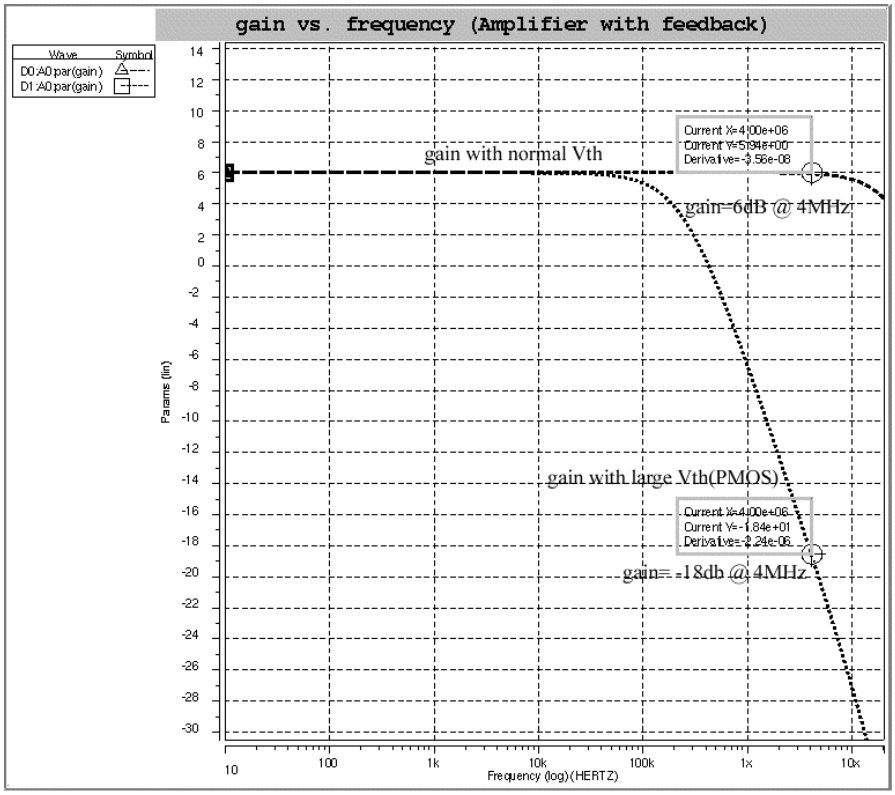


Fig. 36: The frequency response of the amplifier with feedback topology

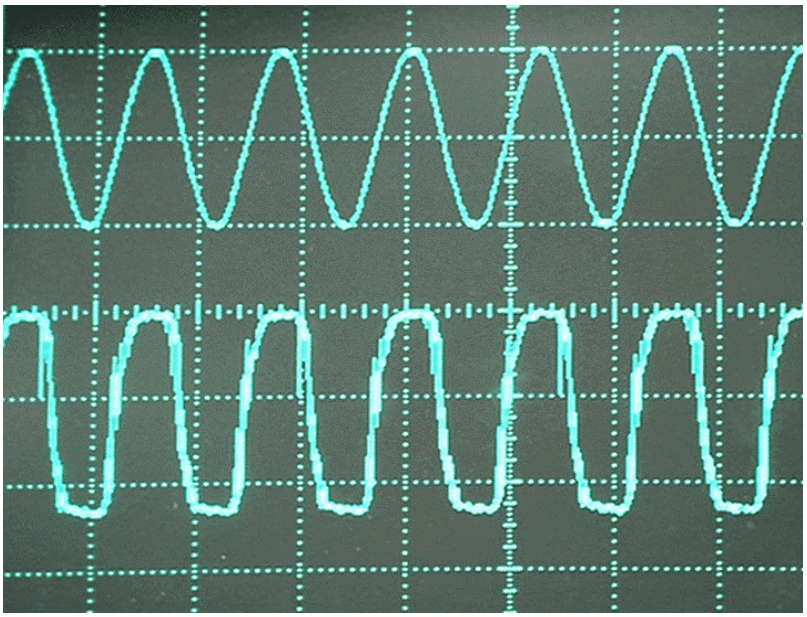


Fig. 37: Measured input and output waveforms of the clock recovery circuitry.

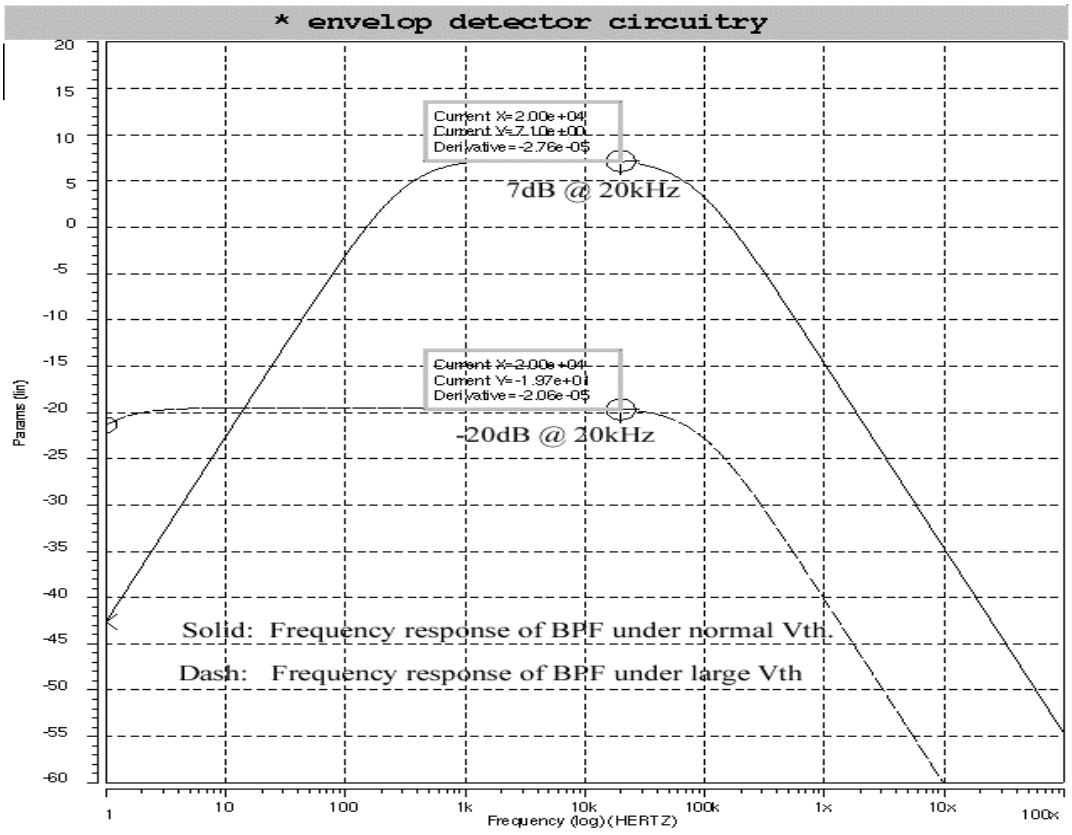


Fig. 38: Frequency response of the envelope detector.

Design Modifications of the Telemetry Circuit Blocks

Because this was the first fabrication run for the MOSIS AMI ABN (1.5μm) process, the parameters, such as the threshold voltage, used to simulate the circuits were much different from the actual threshold voltages of the fabricated chip, especially for PMOS transistors. By considering the large variation of PMOS threshold voltage shown in the new runs, we made some modifications and re-simulated the circuits. Note that the basic circuit topologies were not changed; the only changes made were to make the circuit more tolerant to threshold voltage variations. Figure 39 shows the circuit diagram of the operational amplifier used in the voltage regulator.

It can be seen from Fig. 39 that transistors M8-M16, R, Q1 and Q2 form the self-biased current source for the well-known two-stage amplifier so the bias current of the preamplifier will be insensitive to variations in the power supply and the threshold voltage shifts. Moreover, the cascoded structure (M11-M14) leads to better Power Supply Rejection Ratio (PSRR), further stabilizing the bias current. This circuit structure is also implemented in the amplifier used in the regulator, where the power supply of that amplifier is just the rectified RF signal with large ripples.

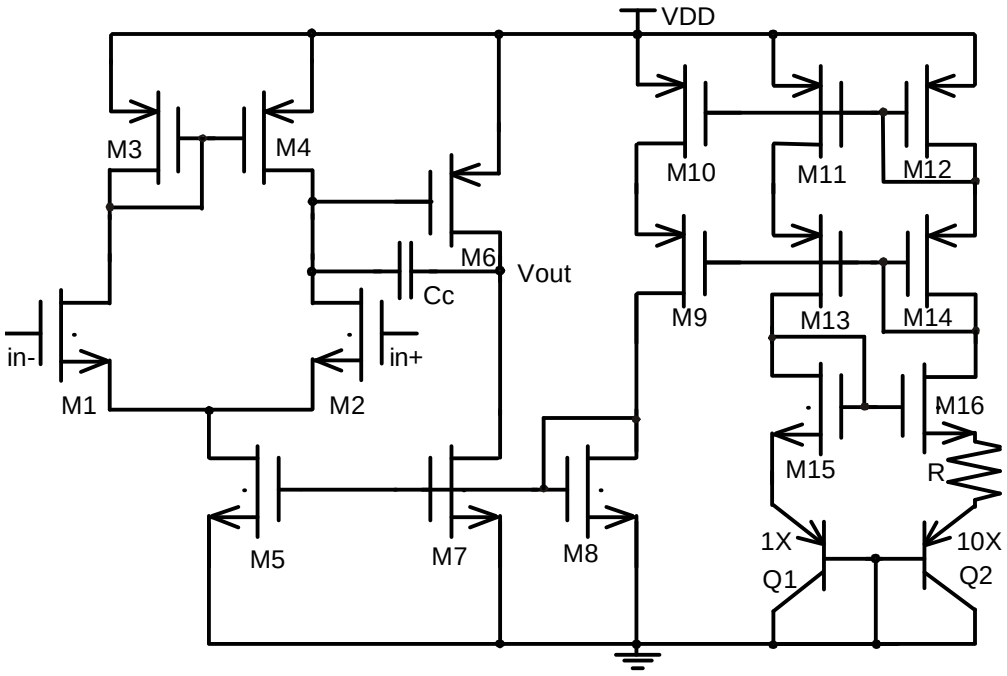


Fig. 39: The schematic of the preamplifier.

The new circuits have been designed and laid out using the AMI ABN process (Lambda = 0.8µm, which is recommended by MOSIS to obtain consistent and uniform electrical behavior for both analog and digital designs). The MOSIS AMI ABN process offers two levels of metal, two levels of polysilicon, and an optional BJT NPN. The two polysilicon layers are used to implement capacitors, and the optional P-base layer is used for optional NPN transistors. In addition, the substrate PNP transistor can used in the bandgap circuitry. Figure 40 shows the layout of the chips sent to MOSIS. The chip measures 1916µm X 1916µm. They are currently in fabrication and are expected to be finished at the beginning of October. Some test devices are also included in this layout in order to obtain more practical parameters for future design and simulations.

8. Conclusions

During the past quarter, we have developed a 1.5µm process for polysilicon definition on our recording probes, reducing the previous feature size by a factor of two. This process has been used in a new mask set containing five probes for acute 3-D cell localization and 2-D current source density analysis in visual cortex. Each probe has 54 sites arranged in two or three rows on a single shank less than 215µm wide.

We are continuing our experiments with a variety of site sizes, placements, and coatings in an effort to improve the lifetime of recording sites in-vivo during chronic implants. We are preparing probes to be implanted during the coming quarter with various biopolymers, including electrodeposited polypyrrole/peptide CDPGYIGSR a

neuronal binding agent), PEG (polyethylene glycol, to decrease protein adsorption and cell attachment), and PEDOT (poly(3,4-ethylenedioxythiophene), which is a conducting polymer based upon thiphene.

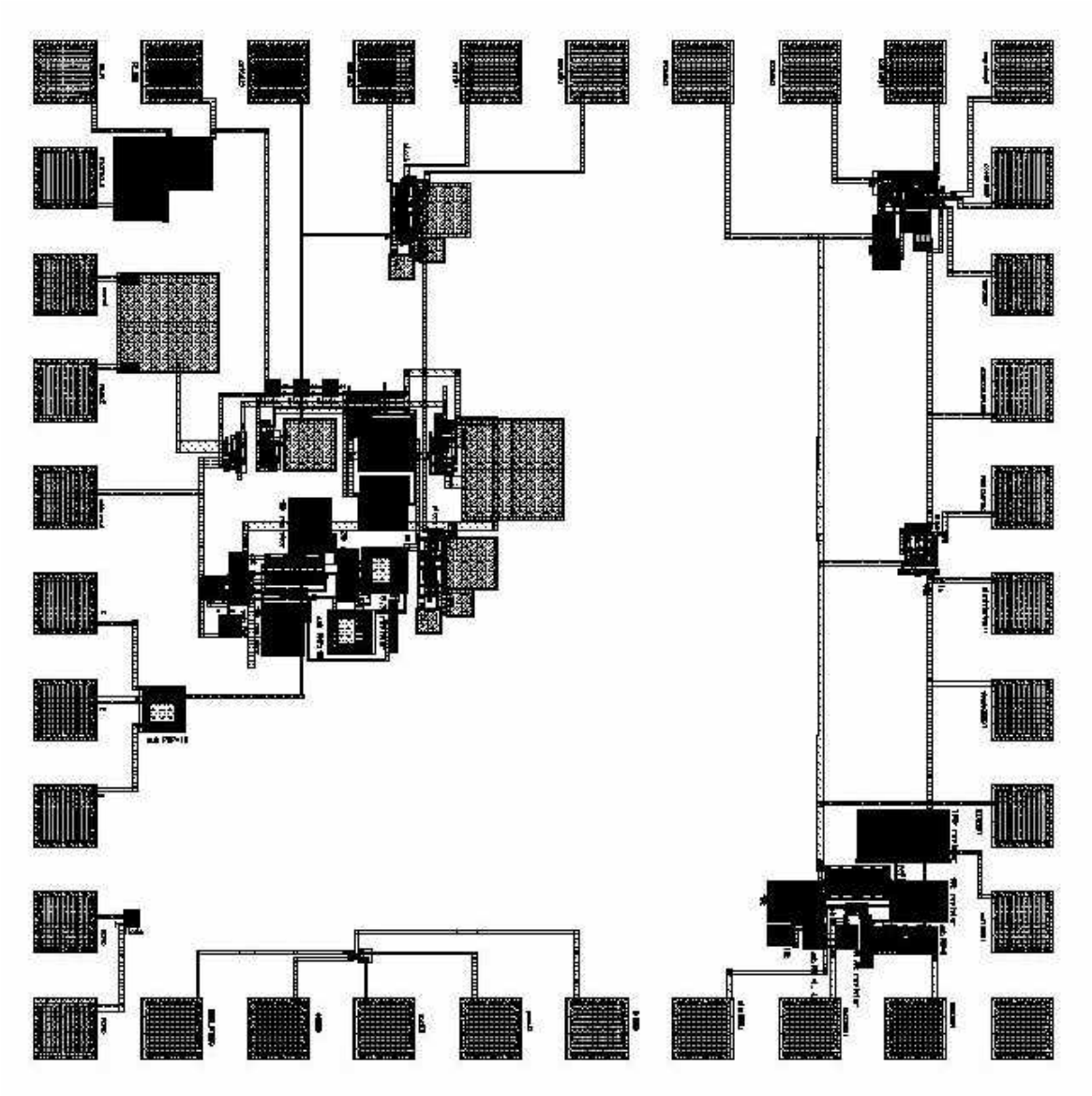


Fig. 40: The layout of the front-end circuits and the preamplifier.

During the past quarter, two chronic probes have been implanted with a variety of site positions on the substrate and with site areas of 1000μm^2 at the tip and 177 μm^2 near the center of the substrate. Currently, the probes have been implanted for eight weeks and two weeks in two different animals. All sites on both probes are currently active, with evidence of single-unit, multi-unit and/or evoked potential activity on every channel. Standard methods are being developed to analyze these waveforms so that differences in site recording capability can be compared from probe to probe and animal to animal. The waveforms are thresholded to extract spikes that exceed four standard deviations above

the total signal average (spikes plus noise). A cluster plot is then constructed using the first two principal components of the total separated spikes, and k-means clustering is used to separate the spikes into single units and eliminate spikes likely to have been caused by noise. Finally, a template (average) waveform is constructed for each separated single unit. The signal-to-noise ratio (SNR) is then defined as the peak-to-peak voltage of the template waveform to the standard deviation of the neural record with spikes extracted. For the two probes implanted thus far, the SNRs for tip sites and center sites have been 6.6 and 6.4 for the day of implant and 5.9 and 4.7 eight weeks after implant. The increased noise seen over time appears to track well with the increase in the real part of the site impedance.

In developing active probes, two new mask sets containing a variety of active probes are now in fabrication. These include a redesigned PIA-2B/-3B as well as probes containing readout circuits that will be used on PIA-2/-3 later this year. The circuits being evaluated on these probes include several amplifiers having gains of approximately 1000 from 10Hz to >10kHz, zero or unity DC gain, power dissipation of <100μW, and areas of <0.1mm^2. The input-referred noise on these circuits is typically less than 7μV-rms. In addition, multiplexer designs are being evaluated. MOSIS chips with the first of the telemetry interface designs were received during the past term and were evaluated. In spite of the fact that the PMOS device thresholds were larger than the design targets provided initially by the foundry, several of these circuits functioned nearly as expected. The circuits have been redesigned to make them more tolerant to process-induced variations and have been resubmitted for fabrication. They are expected back this fall when they will be evaluated at that time.